1995 DATA BOOK MID-YEAR SUPPLEMENT

BENCHMARQ

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1995
Data Book
Mid-Year Supplement

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BENCHMARQ 1995 Data Book Mid-Year Supplement

This data book contains new product information. Benchmarq reserves the right to make changes in its products without notice.

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Our Products

At Benchmarq, we provide integrated circuit and module solutions for power-sensitive and portable electronics systems.

Power-sensitive AC-powered systems in the office and industry must gracefully deal with the loss of power, maintaining the integrity of important data and self-sufficiently continuing critical operation. Portable systems share the design requirements of their powercord-bound counterparts, but add entirely new challenges—including power supervision, energy management, data security, and size minimization.

The product families described in this data book directly address these requirements, taking full advantage of advanced analog and digital VLSI technologies and state-of-the-art battery and packaging expertise. Power supervision, energy management, size reduction, nonvolatility, data security, and retrofit capability are integral to Benchmarq's product line.

Our Commitment

When you choose to integrate Benchmarq products within your own, be assured that Benchmarq is committed to providing the specific solutions you need today and to developing creative solutions to the growing challenges of tomorrow—supported by the best customer service and the highest overall quality.

The drive for excellence in all dimensions of quality is a cornerstone of our company.

Data Book Organization

This mid-year supplement updates information contained in the 1995 Data Book and adds new product information. This supplement and the 1995 Data Book are organized into general information sections and product family sections. The selection guides in Chapter 1 indicate whether the current product data sheet is contained in this supplement or in the 1995 Data Book.

You can locate information in this book in several ways.

To locate information by:	See pages:
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Chapters 2 through 5 contain detailed product information. Chapter 6 includes packaging information, and Chapter 7 describes Benchmarq's commitment to quality and the processes we use to ensure reliability in our products. Chapter 8 lists sales offices and distributors.

For More Information ...

If you haven't found it here . . . Ask!

Benchmarq maintains an updated product listing on the World Wide Web at the URL listed below. Browse the Benchmarq Home Page for the latest Benchmarq product information and sales office locations at:

http://www.benchmarq.com

To send us e-mail to be added to our mailing list or to get further information, contact Benchmarq at:

benchmarq@benchmarq.com

Additional Benchmarq information is available from your Benchmarq distributor or sales office (listed in the back of this Data Book), or by contacting Benchmarq Customer Service at (800) 966-0011 or (214) 437-9195.

Alphanumeric Product Index

Data Sheet Types

Product information data sheets progress in detail as the product goes from design to full production.

The three types of data sheets are defined below.

- Advance Information: Benchmarq Advance Information data sheets provide information for early product planning. These data sheets describe a product in the design or development stage. Specifications may change in any manner.
- Preliminary: Benchmarq Preliminary data sheets provide preliminary specifications for product design. They describe a product through its early production stage. Supplementary data may be published at a later date.
- Final: Benchmarq data sheets not labeled Advance Information or Preliminary are considered Final. They describe a product in full production and provide specifications for product design.

Benchmarq reserves the right to make changes to any products without notice.

Engineering Prototype

Prior to full production, Benchmarq may provide limited quantities of Engineering Prototypes. Engineering Prototypes are suitably tested for evaluation and restricted use. Any necessary errata data accompanies engineering prototype parts. They are marked with the part number and are identified as Engineering Prototypes.

Electrostatic Discharge (ESD) and Integrated Circuit (IC) Handling

Benchmarq ICs, as all ICs, are sensitive to electrostatic discharge (ESD). Although Benchmarq ICs are designed to withstand high ESD voltages, improper handling may cause damage. Standard ESD-prevention handling procedures should be followed. ESD-prevention considerations include proper grounding of operators, work surfaces and chip-handling equipment; appropriately high relative humidity levels; and use of antistatic handling and packaging materials. The ICs should be stored and shipped in antistatic tubes. The antistatic tubes containing the ICs must be brought to the same potential as the work area/operator before the individual ICs are handled.

bq2001 Energy Management Unit™ (EMU™) Summary and Selection Guide

The bq2001 EMU battery-management IC provides a "gas gauge" capacity monitor, fast charge control, and sophisticated battery conditioning for battery-operated electronic systems.

- Gas gauge capability for direct measurement of battery discharge consumption and capacity
- Fast charging and conditioning control for nominal 4.8V–12V nickel cadmium or lead acid batteries
  - Programmed constant charge, pulsed charge, or "burp" charge
  - Full charge detection by negative delta voltage, maximum temperature, maximum voltage, and maximum charge time
- Programmable for adaptive operation
- EEPROM default settings for application-specific configuration
- Programmable open-drain outputs for status indication or control
- Provides battery-backup supply from main battery, switching to backup cell
- Operates directly from 5.5V–18V charging supply or 4.5V–5.5V V_{CC}
- Direct microprocessor bus interface for capacity monitoring

bq2001 EMU Selection Guide

Configuration	Battery Voltage	Operating Supply	Backup Supply Output Voltage	Pins / Package	Part Number	Page Number
Microprocessor peripheral	up to 18V	5.5–18V charging supply or 4.5V–5.5V V_{CC}	2–6V	24 / .300" NDIP, SOIC	bq2001*	2-1

*Last-time buy.

Fast Charge IC Summary and Selection Guide

The Fast Charge IC family provides fast charge control, switch-mode current regulation, and battery conditioning for rechargeable batteries.

- Fast charging and conditioning of nickel cadmium, nickel metal hydride, lead acid, lithium ion, or rechargeable alkaline batteries
- Flexible current regulation:
  - Frequency-modulated switching current regulator for low-heating design
  - Gating control for use with external regulator
- Easily integrated into systems or as a stand-alone charger
- Pre-charge checks for temperature and voltage faults
- Direct LED outputs display battery and charge status
- Fast charge termination by delta temperature/delta time, negative delta voltage, peak voltage detect, maximim voltage/minimum current, maximum temperature, voltage, and time
- Optional top-off charge
- Discharge-before-charge option
- Variable-rate charging uses excess supply current to charge batteries during system operation

Fast Charge IC Selection Guide

Battery Technology	Charge Control Output	Termination Method	Key Features	Pins / Package	Part Number	Page Number
NiMH NiCd	Single	-ΔV, peak voltage, time, and temp. and voltage qual.	Low power and small size	8/.300" DIP, 8/.150" SOIC	bq2002	1995 Data Book
NiMH NiCd	Single	ΔT/Δt, max. temp., time, and temp. and voltage qual.	Low power and small size	8/.300" DIP, 8/.150" SOIC	bq2002T	
NiMH NiCd Lead Acid	Single	-ΔV, ΔT/Δt, max. temp., voltage, and time	Includes PWM	16/.300" DIP, 16/.300" SOIC	bq2003	
NiMH NiCd	Single	-ΔV, peak voltage, ΔT/Δt, max. temp., voltage, and time	PWM and low-power mode	16/.300" DIP, 16/.150" SOIC	bq2004	
NiMH NiCd	Single	-ΔV, peak voltage, ΔT/Δt, max. temp., voltage, and time	PWM, pulsed precharge conditioning	16/.300" DIP, 16/.150" SOIC	bq2004E	
NiMH NiCd	Dual	-ΔV, ΔT/Δt, max. temp., voltage, and time	Sequential charger	20/.300" DIP, 20/.300" SOIC	bq2005	
NiMH NiCd	Single	-ΔV, peak voltage, max. temp, voltage, time	LCD/LED display	24/.300" DIP, 24/.300" SOIC	bq2007	
Lead Acid	Single	max. voltage/min. current, $-\Delta^2V$, temp., and time	Temp. compensated thresholds	16/.300" DIP, 16/.150" SOIC	bq2031	2-59
Lithium Ion	2–4 cells	max. charge and discharge voltage safety cut-off	Very low power	8/.300" DIP, 8/.150" SOIC	bq2053	2-129
Lithium Ion	Single	max. voltage/min current, temp and voltage qual.	Temp. compensated thresholds	16/.300" DIP, 16/.150" SOIC	bq2054	1995 Data Book
Rechargeable Alkaline	2 cells	maximum voltage	Individual cell charging	8/.300" DIP, 8/.150" SOIC	bq2902	2-199
Rechargeable Alkaline	3 or 4 cells	maximum voltage	Individual cell charging	14/.300" DIP, 14/.150" SOIC	bq2903	2-207

Gas Gauge IC Family Summary and Selection Guide

The Gas Gauge IC family measures the available charge, calculates self-discharge, and optionally provides the available charge over a serial port or by directly driving an LED display.

- Conservative and repeatable measurement of available charge for nickel cadmium, nickel metal-hydride, and lithium ion rechargeable batteries
- Designed for battery pack integration
  - 150µA typical operating current
- Integrate within a system or as a stand-alone device
  - Serial port or direct LED display
- Self-discharge calculation compensated using internal temperature sensor
- Measurement compensated for current rate and temperature
- Accurate measures across a wide range of currents
- bq2012/bq2014 charge-control output controlled by measured state-of-charge, temperature, and voltage
- System Management Bus and Smart Battery Data support (bq2040)

Gas Gauge Selection Guide

Configuration	Application	Key Features	Pins / Package	Part Number	Page Number
Battery pack or system integration	General	Low cost, min. components	16 / .300" DIP, 16 / .150" SOIC	bq2010	2-27
Battery pack or system integration	Very high discharge rates (i.e., power tools)	Low cost, min. components	16 / .300" DIP, 16 / .150" SOIC	bq2011	1995 Data Book
Battery pack or system integration	Very high discharge rates (i.e., power tools)	Low cost, min. components	16 / .300" DIP, 16 / .150" SOIC	bq2011J	2-29
Battery pack or system integration	General	Charge control output	16 / .300" DIP, 16 / .150" SOIC	bq2012	1995 Data Book
Battery pack or system integration	General	External charge control support	16 / .300" DIP, 16 / .150" SOIC	bq2014	
Battery pack or system integration	SMBus interface	External E^2 support	16 / .300" DIP, 16 / .150" SOIC	bq2040	2-73
Battery pack or system integration	Li-Ion packs	Capacity in mAh and mWh	16 / .300" DIP, 16 / .150" SOIC	bq2050	2-97

Nonvolatile SRAM Summary and Selection Guide

Benchmarq's NVSRAMs integrate—in a single-DIP package—extremely low standby power SRAM, nonvolatile control circuitry, and a long-life lithium cell. The NVSRAMs combine secure nonvolatility (more than 10 years in the absence of power) with standard SRAM pinouts and fast unlimited read/write operation.

- ➤ Data retention in the absence of power
- ➤ Automatic write-protection during power-up/power-down cycles
- ➤ Industry-standard pinout
- ➤ Conventional SRAM operation; unlimited write cycles
- ➤ 10 or 5 years minimum data retention in the absence of power
- ➤ Battery internally isolated until power is first supplied
- ➤ Industrial temperature range available

Nonvolatile SRAM Selection Guide

Density	Configuration	Technology	Access Time (ns)	Minimum Data-Retention Time	Pins / Package	Part Number[1]	Page Number
64 Kb	8 Kb x 8	NVSRAM	70, 85[2], 150[2], 200	10 years	28 / DIP	bq4010/ bq4010Y	1995 Data Book
256 Kb	32 Kb x 8	NVSRAM	70[2], 100, 150[2], 200	10 years	28 / DIP	bq4011/ bq4011Y	
1 Mb	128 Kb x 8	NVSRAM	70[2], 85[2], 120	10 years	32 / DIP	bq4013/ bq4013Y	
2 Mb	256 Kb x 8	NVSRAM	85, 120	10 years	32 / DIP	bq4014/ bq4014Y	
	128 Kb x 16	NVSRAM	85, 120	10 years	40 / DIP	bq4024/ bq4024Y	
4 Mb	512 Kb x 8	NVSRAM	70, 85, 120	5 or 10 years	32 / DIP	bq4015/ bq4015Y	
	256 Kb x 16	NVSRAM	85, 120	5 years	40 / DIP	bq4025/ bq4025Y	
4 Mb	512 Kb x 8	NVPSRAM	150[3]	10 years[3]	40 / DIP	bq4115Y	
8Mb	1024 Kb x 8	NVSRAM	70	10 years	36 / DIP	bq4016 bq4016Y	5-1
16Mb	2048 Kb x 8	NVSRAM	70	5 years	36 / DIP	bq4017 bq4017Y	5-11

Notes:
1. "Y" version denotes 10% V_{CC} tolerance.
2. "Y" version available in -40°C to +85°C industrial temperature range.
3. See data sheet for details.

Benchmarq's nonvolatile controllers provide power monitoring, write-protection, and supply switching to convert standard SRAM or PSRAM and a backup battery into a reliable, predictable nonvolatile memory. The nonvolatile controller modules are complete battery-backup solutions including an encapsulated 130mAh lithium cell that is isolated until power is applied.

- Power monitoring and switching for 3V battery-backup applications
- 5V or 3V Vcc operation
- Automatic write-protection during power-up/power-down cycles
- Automatic switching from Vcc to first backup battery and from first backup battery to second backup battery
- Reset output option for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation
- Control up to four banks of SRAM
- Module/DIP or SOIC packages

Nonvolatile Controller Selection Guide

SRAM Banks Controlled	Battery Monitor Outputs	Reset Output	I_{OUT} (Typ.)	Pins / Package	Part Number	Page Number
1			160 mA	8 / NDIP, NSOIC	bq2201	1995 Data Book
2		✓	160 mA	16 / NDIP, NSOIC	bq2202	
2	✓	✓	160 mA	16 / NDIP, NSOIC	bq2203A	
4			160 mA	16 / NDIP, NSOIC	bq2204A	
2		✓	80 mA	16 / NDIP, NSOIC	bq2212	
2		✓	160 mA	12 / DIP module	bq2502	

Real-Time Clock Summary and Selection Guide

Benchmarq's family of real-time clocks (RTCs) provide highly integrated clock/calendar solutions for microcomputer-based designs. Each *module* is a completely self-contained unit, including IC, crystal, and a battery ensuring operation for 10 years in the absence of power. The very compact, low-power *ICs* need only a battery and a crystal for operation. NVSRAM controller versions allow users to make inexpensive SRAM nonvolatile for data and configuration storage in computers, portable equipment, office machines and other applications.

- ➤ Clock/calendar counts seconds through years with daylight savings and leap-year adjustments
- ➤ IBM PC AT-compatible clocks include:
  - 5- or 3-Volt operation
  - 114 or 242 bytes of user nonvolatile RAM storage
  - 32KHz output for power management
- ➤ SRAM-based clocks feature:
  - SRAM interface
  - Up to 128Kbytes of NVSRAM
  - CPU Supervisor
- ➤ Completely self-contained modules operate for more than 10 years in the absence of power
- ➤ IC versions require only a crystal and battery
- ➤ One minute per month clock accuracy in modules
- ➤ Nonvolatile control for an external SRAM

Real-Time Clock Selection Guide

Onboard RAM (bytes)	NVRAM Control	Bus Interface	Voltage	32kHz Output	CPU Super-visor	Pins / Package	Part Number	Page Number
114		Muxed	5V			24 / DIP, SOIC 28 / PLCC	bq3285	1995 Data Book
242		Muxed	5V	✓		24 / DIP, SOIC, SSOP 28 / PLCC	bq3285E	
242		Muxed	3V	✓		24 / DIP, SOIC, SSOP	bq3285L	
114		Muxed	5V			24 / DIP module	bq3287/ bq3287A	
242		Muxed	5V	✓		24 / DIP module	bq3287E/ bq3287EA	
114	✓	Muxed	5V			24 / DIP, SOIC 28 / PLCC	bq4285	
114	✓	Muxed	5V	3		24 / DIP, SOIC, SSOP, 28 / PLCC	bq4285E	
114	✓	Muxed	3V	3		24 / DIP, SOIC,SSOP	bq4285L	
114	✓	Muxed	5V			24 / DIP module	bq4287	
114	✓	Muxed	5V	3		24 / DIP module	bq4287E	4-1
32K		SRAM	5V			28 / DIP module	bq4830Y	1995 Data Book
32K		SRAM	5V		✓	32 / DIP module	bq4832Y	
128K		SRAM	5V		✓	32 / DIP module	bq4842Y	
0	✓	SRAM	5V		3	28 / DIP, SOIC	bq4845/Y	
0	✓	SRAM	5V		3	28 / DIP module	bq4847/Y	

NVSRAM Cross-Reference

Density	Dallas Semiconductor	SGS-Thomson	Benchmarq
64Kb	DS1225AB DS1225AD/Y	MK48Z08 MK48Z18	bq4010 bq4010Y
256Kb	DS1230AB DS1230Y DS1630AB DS1630Y	M48Z30 M48Z30Y - -	bq4011 bq4011Y Contact factory Contact factory
1Mb	DS1245AB DS1245Y DS1645AB DS1645Y DS1645EE	M48Z128 M48Z128Y - - -	bq4013 bq4013Y Contact factory Contact factory Contact factory
2Mb	- - DS1658AB DS1658Y	M48Z256 M48Z256Y M46Z128 M46Z128Y	bq4014 bq4014Y bq4024 bq4024Y
4Mb	DS1650 DS1650Y - -	M48Z512 M48Z512Y M46Z256 M46Z256Y	bq4015 bq4015Y bq4025 bq4025Y

Real-Time Clock Cross-Reference

Dallas Semiconductor	SGS-Thomson	Motorola[1]	Benchmarq
DS1285/885	-	MC146818AP MC146818BP	bq3285P
DS1285Q/885Q	-	MC146818FN	bq3285Q
DS1285S/885S	-	MC146818SP	bq3285S
DS1287/887	MK48T87B24	MC146818BM	bq3287MT
DS1287A/887A	-	MC146818B1M	bq3287AMT
DS1643Y	M48T18	-	bq4830Y[2]
DS1644Y	-	-	bq4830Y

Notes:

1. Last-time buy in progress—obsolete device.
2. Memory upgrade

Nonvolatile Controllers Cross-Reference

Dallas Semiconductor	Benchmarq
DS1210	bq2201PN [4]
DS1210S	bq2201SN [1, 4]
DS1221	bq2204APN [3, 4]
DS1221S	bq2204ASN [2, 3, 4]

Notes:

1. Benchmarq's bq2201SN is a small 8-pin, 150-mil SOIC, compared to the DS1210S, which is a 16-pin, 300-mil SOIC.
2. Benchmarq's bq2204ASN is a small 16-pin, 150-mil SOIC, compared to the DS1221S, which is a 16-pin, 300-mil SOIC.
3. Optional "security feature" DS1221 pins are no-connect on the bq2204A.
4. Benchmarq's bq2201 and bq2204A do not incorporate a "check battery status" function.

Benchmarq's standard products are available in several packages and operating ranges. A valid order number is a sequence of:

- Device
- Package Options
- Speed Options
- Temperature Range

Valid options for a specific device are defined in the ordering information section at the end of its data sheet. Contact your Benchmarq sales office about non-standard requirements or to place an order. Sales offices are listed at the end of this data book.

bq40xx MA - __ __

Temperature Range:

blank	= Commercial (0 to +70°C)
I	= Extended (–20 to +70°C)
N	= Industrial (–40 to +85°C)

Speed Options:

70, 85, ... , 200, or blank

Package Options:

P	= Plastic DIP
PN	= Narrow Plastic DIP
S	= SOIC
SN	= Narrow SOIC
SS	= SSOP
Q	= Quad PLCC
Mx	= x-type module

Device:

bq2003
bq2201
bq4011Y
bq4287
etc.

Examples:

bq2003S
bq2201SN-N
bq2204PN-N
bq4010YMA-150N
bq4011MA-100
bq4287MT

Notes

Energy Management Unit (EMU)

Features

- Microprocessor peripheral for battery management and related functions
- Direct measurement of battery charge consumption and capacity
- Fast charging and conditioning control for nominal 4.8V to 12V nickel cadmium, lead acid, or nickel hydride batteries
- Full-charge detection by negative delta voltage method, maximum temperature, maximum voltage, and maximum time
- Programmable for adaptive operation
- EEPROM default settings for application-specific configuration
- Open-drain outputs for status indication or control
- Provides and controls 3V battery-backup supply
- Operates from 5.5–18V DC or 4.5–5.5V Vcc supplies

General Description

The BiCMOS bq2001 Energy Management Unit (EMU) is a low-power microprocessor peripheral providing battery-management services for systems using rechargeable (secondary) batteries. The bq2001 works directly from the DC charging supply, operating as programmed, or from 5V Vcc, operating as a microprocessor peripheral. bq2001-based systems can easily incorporate sophisticated capacity monitoring, battery management, backup supply service, and power-conservation capabilities.

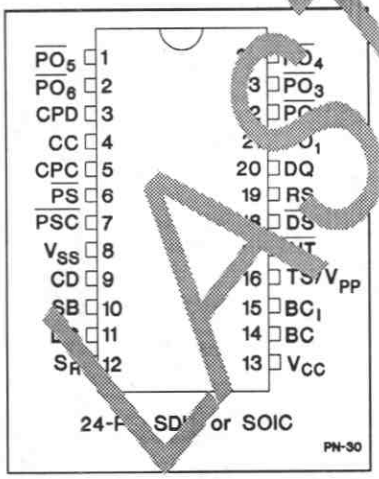
The "gas gauge" register provides the actual charge consumption from the secondary battery and measures the actual battery capacity. The charge time register allows calculation of the energy stored following partial or complete recharge. The programmed end-of-discharge voltage (EDV) threshold determines full discharge.

Battery management includes charge control as standard to fast charge rates, with full charge determination using the preferred negative delta voltage (-ΔV method, a maximum temperature threshold, a maximum voltage threshold, and a maximum time limit. The EMU may also be configured to inhibit or abort charging when the battery temperature is below an acceptable temperature range. Trickle charge can occur before and after charging. Normal operational discharge before charge may be selected for cell conditioning or capacity measurement. Charge pattern may be programmed to be constant, pulsed, or "burp" (alternating charge/discharge).

For the power-off condition, the bq2001 regulates the secondary battery input to maintain its programmed state while it simultaneously sources a backup cell output to maintain a real-time clock or other low-current battery-backed ICs. A backup cell provides system data retention current when the secondary battery is depleted or removed.

System design is simplified by six open-drain outputs controlled by the EMU or the host processor. These may be allocated for subsystem control, LED activation, EMU status indication, and system power switch control.

Pin Connections



Pin Names

$\overline{DS}$	Data strobe input
RS	Register select input
DQ	Data input/output
$\overline{IN}$	Interrupt request output
Vcc	+5V system supply input
DC	Charging supply input
BC	Backup cell output
BCI	Backup cell input
SB	Secondary battery input
SR	Sense resistor input
CC	Charge control output
CPC	Charge pump capacitor output
CPD	Charge pump diode output
CD	Discharge control output
TS/VPP	Temperature sensor input or programming voltage input
$\overline{PS}$	Power switch input
$\overline{PSC}$	Power switch control output
$\overline{PO_1}$	Charging indicator or programmable output 1
$\overline{PO_2}$	End-of-discharge voltage indicator or programmable output 2
$\overline{PO_3}$	Temp not OK indicator or programmable output 3
$\overline{PO_4}$	DC valid indicator or programmable output 4
$\overline{PO_5}$	Gas gauge threshold indicator or programmable output 5
$\overline{PO_6}$	Secondary battery fault or programmable output 6
VSS	System ground

bq2001 Last Time Buy Notice

Products Included

Due to a lack of demand, the following products are on a last time buy:

- Battery Management
  - bq2001S
  - bq2001PN

Schedule

Benchmarq will accept orders for these devices through the end of December 1995 with shipments through the end of December 1996.

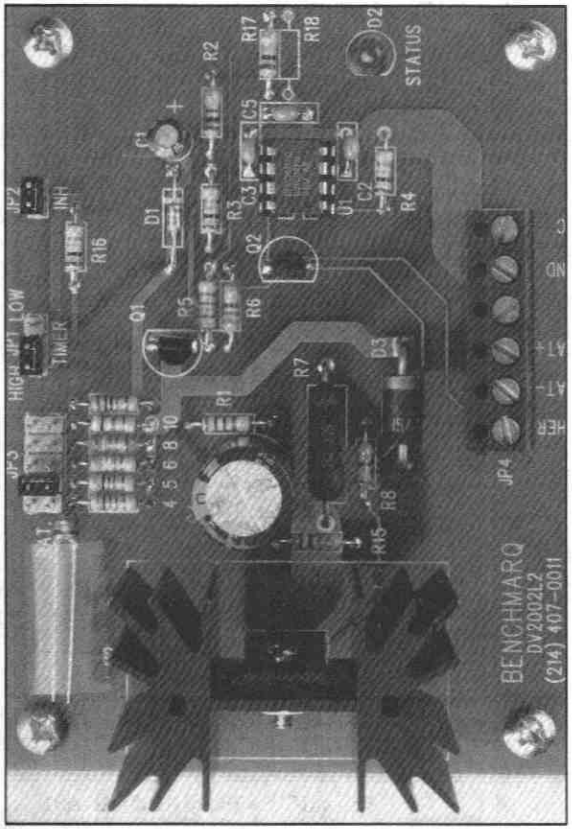
DV2002L2

Fast Charge Development System

Control of LM317 Linear Regulator

Features

- bq2002 fast charge control evaluation and development
- Charge current sourced from an on-board linear regulator (up to 1.5 A)
- Fast charge of 4, 5, 6, 8, or 10 NiCd or NiMH cells (contact Benchmarq for other number of cells)
- Fast charge termination by negative delta voltage (-ΔV) or peak voltage detect, maximum temperature and maximum time
- -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Inhibit fast charge by logic-level input



General Description

The DV2002L2 Development System provides a development environment for the bq2002 Fast Charge IC. The DV2002L2 incorporates a bq2002 and a linear regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: -ΔV or peak voltage detect, maximum temperature, maximum time, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2002L2 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off).

Please review the bq2002 data sheet before using the DV2002L2 board.

Connection Descriptions

JP4

TH	Thermistor connection
BAT+	Positive battery terminal
BAT–	Battery ground
GND	Ground from charger supply
DC	DC input from charger supply

JP3 NOC Select number of cells

JP2 INH Inhibit input

JP1 TM Timer, etc. setting

Fixed Configuration

The DV2002L2 board has the following fixed characteristics :

Vcc (4.75–5.25V) is regulated on-board from the supply at connector JP4 (DC: GND).

$\overline{\text{LED}}$ indicates charge status.

Charge initiates on the later application of the battery or DC, which provides V_{CC} to the bq2002.

As shipped from Benchmarq, the DV2002L2 linear regulator is configured to a charging current of 1.25A. This current level is controlled by the value of sense resistor R_{SNS} by the relationship:

$$I_{CHG} = \frac{1.25V}{R_7}$$

The value of R_7 at shipment is 1Ω. This resistor can be changed depending on the application.

The suggested maximum I_{CHG} for the DV2002L2 board is 1.5A. ***U2 must be mounted to an appropriate heat sink.***

The maximum cell voltage (MCV) is scaled to 2V/cell.

With the provided NTC thermistor connected between TH and BAT–, TCO = 50°C.

Table 1. Lookup Table for R7 Selection

Input Voltage	Current	Resistance	Wattage
to 25V	1A	1.25Ω	2W
	1.5A	0.83Ω	2W

The thermistor is identified by the serial number suffix as follows:

Identifier	Thermistor
K1	Keystone RL0703-5744-103-S1
(blank)	Philips 2322-640-63103
F1	Fenwal Type 16, 197-103LA6-A01
O1	Ozhumi 150-108-00(4)
S1	Semetic 103AT-2

Jumper-Selectable Configuration

The DV2002L2 must be configured as described below.

INH (JP2): Enables/disables charge inhibit (see bq2002 data sheet).

Jumper Setting	Pin State
[1 2] 3	Disabled (high)
1 [2 3]	Enabled (low)

TM (JP1): Selects fast charge safety time/hold-off/top-off (see bq2002 data sheet).

Jumper Setting	Pin State
[1 2] 3	High
1 [2 3]	Low
1 2 3	Float

Number of Cells (JP3): A resistor-divider network is provided to select 4 to 10 cells (the resulting resistor value equals N – 1 cells). RB1 is a 100KΩ resistor, and RB2 (RB20–RB25) is jumper-selected.

Closed Jumper	Number of Cells
R13	10
R12	8
R11	6
R10	5
R9	4

Temperature Disable: Connecting a 10KΩ resistor between TH and BAT– disables temperature control.

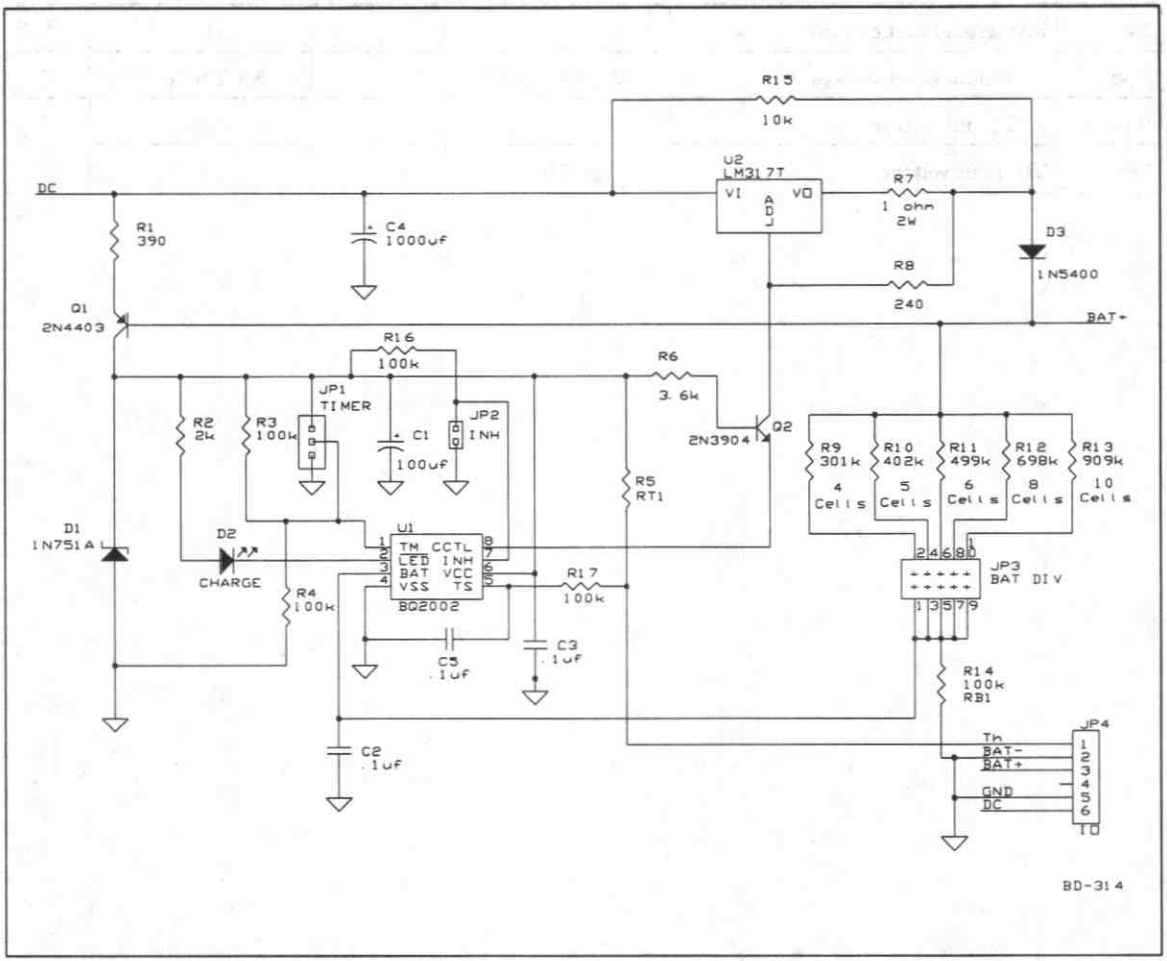
Setup Procedure

1. Configure TM, INH, and number-of-cells (NOC) jumpers.
2. Connect the provided thermistor or a 10KΩ resistor between TH and BAT–.
3. Attach the battery pack to BAT+ and BAT–. For temperature control, the thermistor must contact the cells.
4. Attach DC current source to DC (+) and GND (–) connections in JP4.

Recommended DC Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit
I_{DC}	Maximum input current	-	-	1.5	A
V_{DC}	Maximum input voltage	2.0 + V_{BAT} or 8.5	-	18 + V_{BAT} or 25	V
V_{BAT}	BAT input voltage	-	-	24	V
V_{TH}	TH input voltage	0.5	-	5	V

DV2002L2 Board Schematic



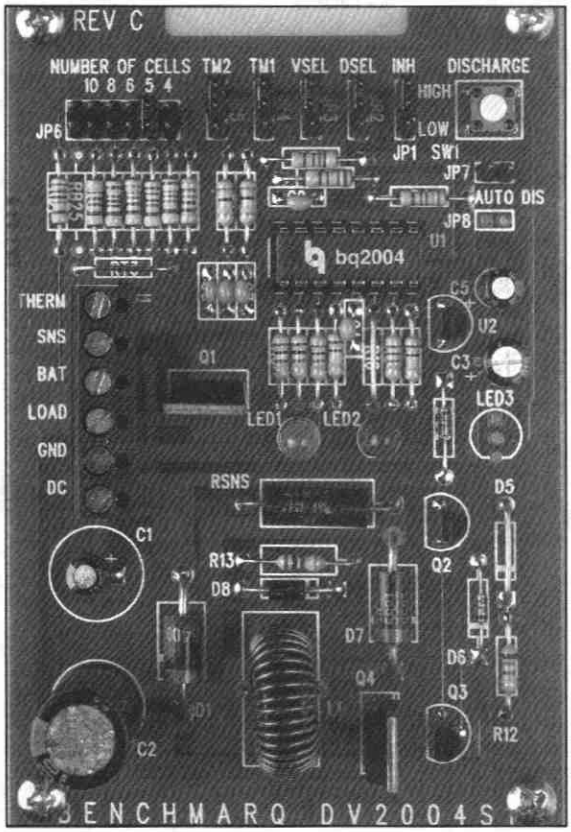
DV2004S1

Fast Charge Development System

Control of On-Board p-FET Switch-Mode Regulator

Features

- bq2004 fast charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 3.0 A)
- Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast charge termination by delta temperature/delta time (ΔT/Δt), negative delta voltage (-ΔV) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input



General Description

The DV2004S1 Development System provides a development environment for the bq2004 Fast Charge IC. The DV2004S1 incorporates a bq2004 and a buck-type switch-mode regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: ΔT/Δt, -ΔV or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

The user provides a power supply and batteries. The user configures the DV2004S1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands discharge-before-charge with push-button switch S1.

Please review the bq2004 data sheet before using the DV2004S1 board.

Connection Descriptions

J1

THERM	Thermistor connection
SNS	Negative battery terminal and thermistor connection
BAT+	Positive battery terminal and high side of discharge load
LOAD	Low side of discharge load
GND	Ground from charger supply
DC	DC input from charger supply

JP1	$\overline{INH}$	Inhibit input
JP2	DSEL	Display select
JP3	VSEL	Voltage termination select
JP4	TM1	TM1 setting
JP5	TM2	TM2 setting
JP6	NOC	Select number of cells
JP7		Auto discharge-before-charge select
JP8		Auto cycle select

Fixed Configuration

The DV2004S1 board has the following fixed characteristics:

V_{CC} (4.75–5.25V) is regulated on-board from the supply at connector J1 DC.

LED1 and LED2 indicate charge status.

LED3 can replace LED1 and LED2 and provide an optional tri-color LED feature.

Charge initiates on the later application of the battery or DC, which provides V_{CC} to the bq2004.

Pin $\overline{DCMD}$ may be tied to ground through JP7 for automatic discharge-before-charge. With JP7 open, a toggle of switch S1 momentarily pulls $\overline{DCMD}$ low and initiates a discharge-before-charge. The bq2004 output activates FET Q1, allowing current to flow through an external current-limiting load between BAT+ and LOAD on connector J1.

As shipped from Benchmarq, the DV2004S1 buck-type switch-mode regulator is configured to a charging current of 2.25A. This current level is controlled by the value of sense resistor R_{SNS} by the relationship:

$$I_{CHG} = \frac{0.225V}{R_{SNS}}$$

The value of R_{SNS} at shipment is 0.100Ω. This resistor can be changed depending on the application.

The suggested maximum I_{CHG} for the DV2004S1 board is 3A. The maximum cell voltage (MCV) setting is 1.8V.

Zener diode D5 is used to limit Q4 V_{GS} per a given DC voltage. The board is shipped with D5 shorted. The user can modify this Zener diode for the application. Refer to Table 1 for suggested D5 values for DC voltages.

Table 1. Lookup Table for D5 Selection

+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

Note: Capacitors C2 and C3 must be changed from those shipped with the board for input voltage in excess of 24V.

With the provided NTC thermistor connected between THERM and SNS, values are: LTF = 10°C, HTF = 45°C, and TCO = 50°C. The $\Delta T/\Delta t$ settings at 30°C ($T_{\Delta T}$) are: minimum = 0.82°C/minute, typical = 1.10°C/minute.

The thermistor is identified by the serial number suffix as follows:

Identifier	Thermistor
K1	Keystone RL0703-5744-103-S1
(blank)	Philips 2322-640-63103
F1	Fenwal Type 16, 197-103LA6-A01
O1	Ozhumi 150-108-00(4)
S1	Semetic 103AT-2

Jumper-Selectable Configuration

The DV2004S1 must be configured as described below.

$\overline{INH}$ (JP1): Enables/disables charge inhibit (see bq2004 data sheet, page 8).

Jumper Setting	Pin State
[1 2] 3	Disabled (high)
1 [2 3]	Enabled (low)

TM1 and TM2 (JP4 and JP5): Select fast charge safety time/hold-off/top-off (see bq2004 data sheet, page 7).

Jumper Setting	Pin State
[1 2] 3	High
1 [2 3]	Low
1 2 3	Float

Number of Cells (JP6): A resistor-divider network is provided to select 4 to 10 cells (the resulting resistor value equals N/2 – 1 cells). RB1 is a 150KΩ resistor, and RB2 (RB20–RB25) is jumper-selected.

Closed Jumper	Number of Cells
RB25	User-selectable
RB24	10
RB23	8
RB22	6
RB21	5
RB20	4

Temperature Disable: Connecting a 10KΩ resistor between THERM and SNS disables temperature control.

DSEL (JP2): Selects LED1 and LED2 (LED3 optional) display state (see bq2004 data sheet, Table 2, page 5).

VSEL (JP3): Selects -ΔV or peak-voltage detection, or disables voltage-based termination (see bq2004 data sheet, page 7).

AUTO DIS SELECT (JP7): Jumping JP7 enables automatic discharge-before-charge.

AUTO CYCLE SELECT (JP8): Jumping JP8 automatically initiates a continuous discharge-before-charge/fast charge cycling for data collection purposes.

Setup Procedure

1. Configure VSEL, TM1, TM2, DSEL, $\overline{INH}$, and number-of-cells (NOC) jumpers.
2. Connect the provided thermistor or a 10KΩ resistor between THERM and SNS.
3. If using the discharge-before-charge or auto-cycle options, connect a current-limiting discharge load between BAT+ and LOAD.
4. Attach the battery pack to BAT+ and SNS. For temperature control, the thermistor must contact the cells.
5. Attach DC current source to DC (+) and GND (–) connections in J1.

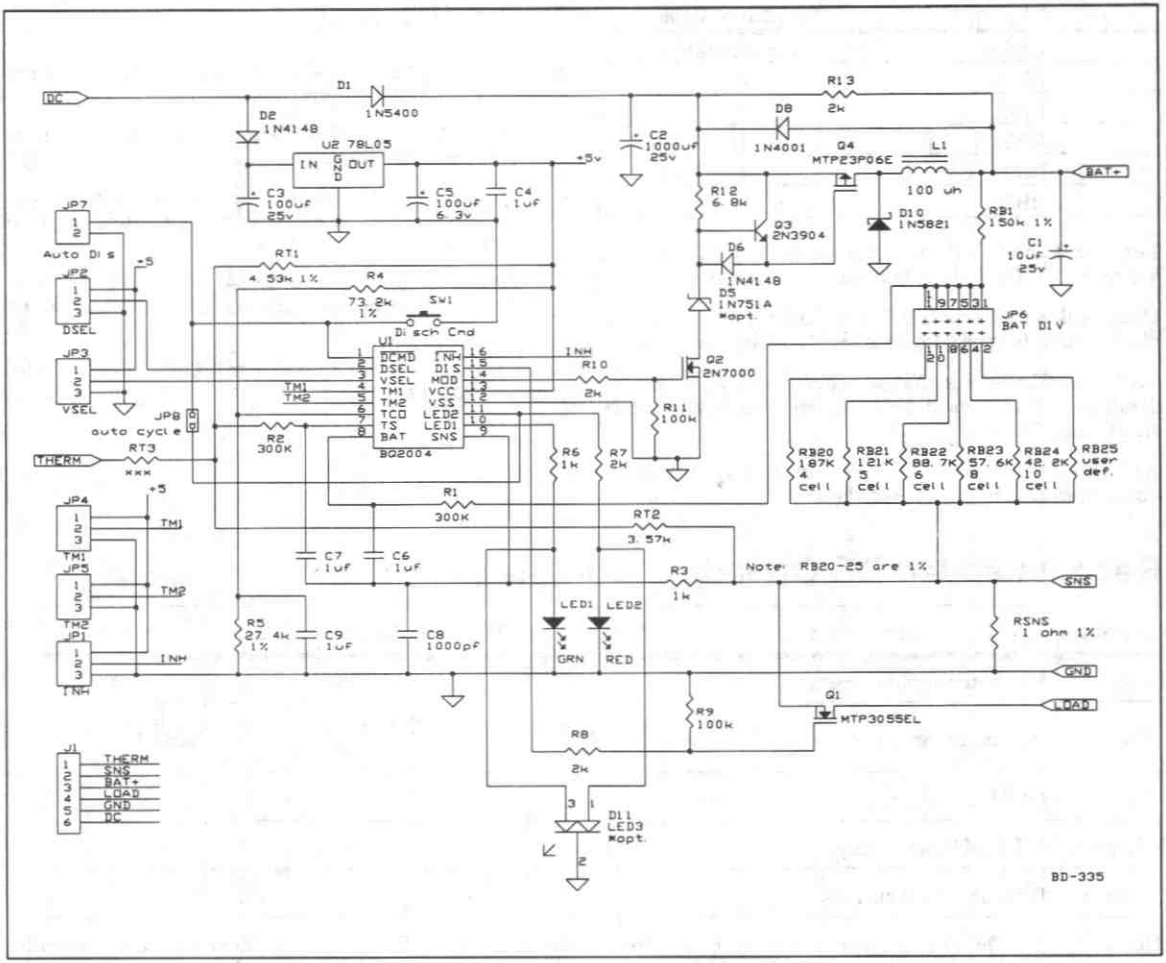
2

Recommended DC Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
I_{DC}	Maximum input current	-	-	2.4	A	
V_{DC}	Maximum input voltage	2.0 + V_{BAT} or 15	-	18 + V_{BAT} or 35	V	Note 1
V_{BAT}	BAT input voltage	-	-	24	V	
V_{THERM}	THERM input voltage	0	-	5	V	
I_{DSCHG}	Discharge load current	-	-	2	A	

Note: 1. The V_{DC+} limits consider the appropriate Zener diode at D5. The voltage at D5 is application-specific and limits the V_{GS} of Q4 to a safe enhancement value during Q4 conduction. See Table 1 for recommended D5 selections per V_{DC+}.

DV2004S1 Board Schematic



BENCHMARQ

Preliminary **DV2004S3**

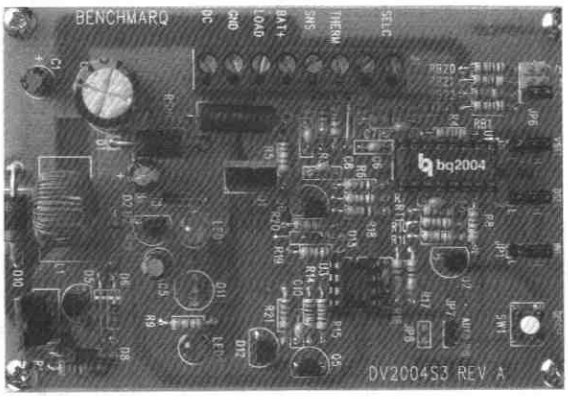
Nickel/Li-Ion Development System

Control of On-Board p-FET Switch-Mode Regulator

2

Features

- bq2004 fast charge control evaluation and development for NiMH, NiCd and Li-Ion
- Charge current sourced from an on-board switch-mode regulator (up to 2.0 A)
- Fast charge of 3, 6, or 9 NiCd or NiMH cells and 1, 2, or 3 Li-Ion cells
- Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage for Nickel-based and constant-current to constant-voltage for Li-Ion
- $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input



General Description

The DV2004S3 Development System provides a dual-chemistry development environment for the bq2004 Fast Charge IC. The DV2004S3 incorporates a bq2004 and a buck-type switch-mode regulator to provide fast charge control for 3, 6, or 9 NiCd or NiMH cells and 1, 2, or 3 Li-Ion cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$ or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

Fast charge for Li-Ion transitions from a constant-current to constant-voltage regulation. Voltage is regulated to within 1%. Charge complete is indicated at the maximum charge time.

The user provides a power supply and batteries. The user configures the DV2004S3 for the number of cells and charge termination mode, and commands discharge-before-charge with push-button switch S1.

Please review the bq2004 data sheet and application note: *Applications Using Nickel-base and Li-Ion Battery Chemistries*, before using the DV2004S3 board.

Connection Descriptions

J1

SELC	Chemistry select
THERM	Thermistor connection
SNS	Negative battery terminal and thermistor connection
BAT+	Positive battery terminal and high side of discharge load

	LOAD	Low side of discharge load
	GND	Ground from charger supply
	DC	DC input from charger supply
JP1	$\overline{\text{INH}}$	Inhibit input
JP2	DSEL	Display select
JP3	VSEL	Voltage termination select
JP6	NOC	Select number of cells
JP7		Auto discharge-before-charge select
JP8		Auto cycle select

Fixed Configuration

The DV2004S3 board has the following fixed characteristics:

V_{CC} (4.75–5.25V) is regulated on-board from the supply at connector J1 DC.

LED1 and LED2 indicate charge status.

LED3 can replace LED1 and LED2 and provides an optional tri-color LED feature

Charge initiates on the later application of the battery or DC, which provides V_{CC} to the bq2004.

Pin $\overline{\text{DCMD}}$ may be tied to ground through JP7 for automatic discharge-before-charge. With JP7 open, a toggle of switch S1 momentarily pulls $\overline{\text{DCMD}}$ low and initiates a discharge-before-charge. The bq2004 output activates FET Q1, allowing current to flow through an external current-limiting load between BAT+ and LOAD on connector J1.

As shipped from Benchmarq, the DV2004S3 buck-type switch-mode regulator is configured to a charging current of 1.5A. This current level is controlled by the value of sense resistor R_{SNS} by the relationship:

$$I_{CHG} = \frac{0.225V}{R_{SNS}}$$

The inductor is configured for a maximum of 1.5 Amp and should not be adjusted without consulting Benchmarq.

Zener diode D5 is used to limit Q4 V_{GS} per a given DC voltage. The board is shipped with D5 shorted. The user can modify this Zener diode for the application. Refer to Table 1 for suggested D5 values for DC voltages.

Table 1. Lookup Table for D5 Selection

+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

Note: Capacitors C2 and C3 must be changed from those shipped with the board for input voltage in excess of 24V.

With the provided NTC thermistor connected between THERM and SNS, values are: LTF = 10°C, HTF = 49°C, and TCO = 50°C. The $\Delta T/\Delta t$ settings at 30°C ($T_{\Delta T}$) are: minimum = 0.82°C/minute, typical = 1.10°C/minute.

The thermistor is identified by the serial number suffix as follows:

Identifier	Thermistor
K1	Keystone RL0703-5744-103-S1
(blank)	Philips 2322-640-63103
F1	Fenwal Type 16, 197-103LA6-A01
O1	Ozhumi 150-108-00(4)
S1	Semetic 103AT-2

Jumper-Selectable Configuration

The DV2004S3 must be configured as described below.

INH (JP1): Enables/disables charge inhibit (see bq2004 data sheet, page 8).

Jumper Setting	Pin State
[1 2] 3	Disabled (high)
1 [2 3]	Enabled (low)

Number of Cells (JP6): A resistor-divider network is provided to select 3, 6, or 9 cells (the resulting resistor value equals N/2 – 1 cells).

Closed Jumper	Number of Cells	
	NiCd/NiMH	Li-Ion
RB22	9	3
RB21	6	2
RB20	3	1

Temperature Disable: Connecting a 10KΩ resistor between THERM and SNS disables temperature control.

DSEL (JP2): Selects LED1 and LED2 (LED3 optional) display state (see bq2004 data sheet, Table 2, page 5).

VSEL (JP3): Selects -ΔV or peak-voltage detection, or disables voltage-based termination (see bq2004 data sheet, page 7).

AUTO DIS SELECT (JP7): Jumping JP7 enables automatic discharge-before-charge.

AUTO CYCLE SELECT (JP8): Jumping JP8 automatically initiates a continuous discharge-before-charge/fast charge cycling for data collection purposes.

Setup Procedure

1. Configure VSEL, TM1, TM2, DSEL, $\overline{INH}$, and number-of-cells (NOC) jumpers.
2. Connect the provided thermistor or a 10KΩ resistor between THERM and SNS.
3. If using the discharge-before-charge option, connect a current-limiting discharge load between BAT+ and LOAD.
4. For a Nickel-based battery, attach the battery pack to BAT+, SNS, and THERM. SELC should float. For Li-Ion, SELC must be connected to BAT+ to operate properly.
5. Attach DC current source to DC (+) and GND (–) connections in J1.

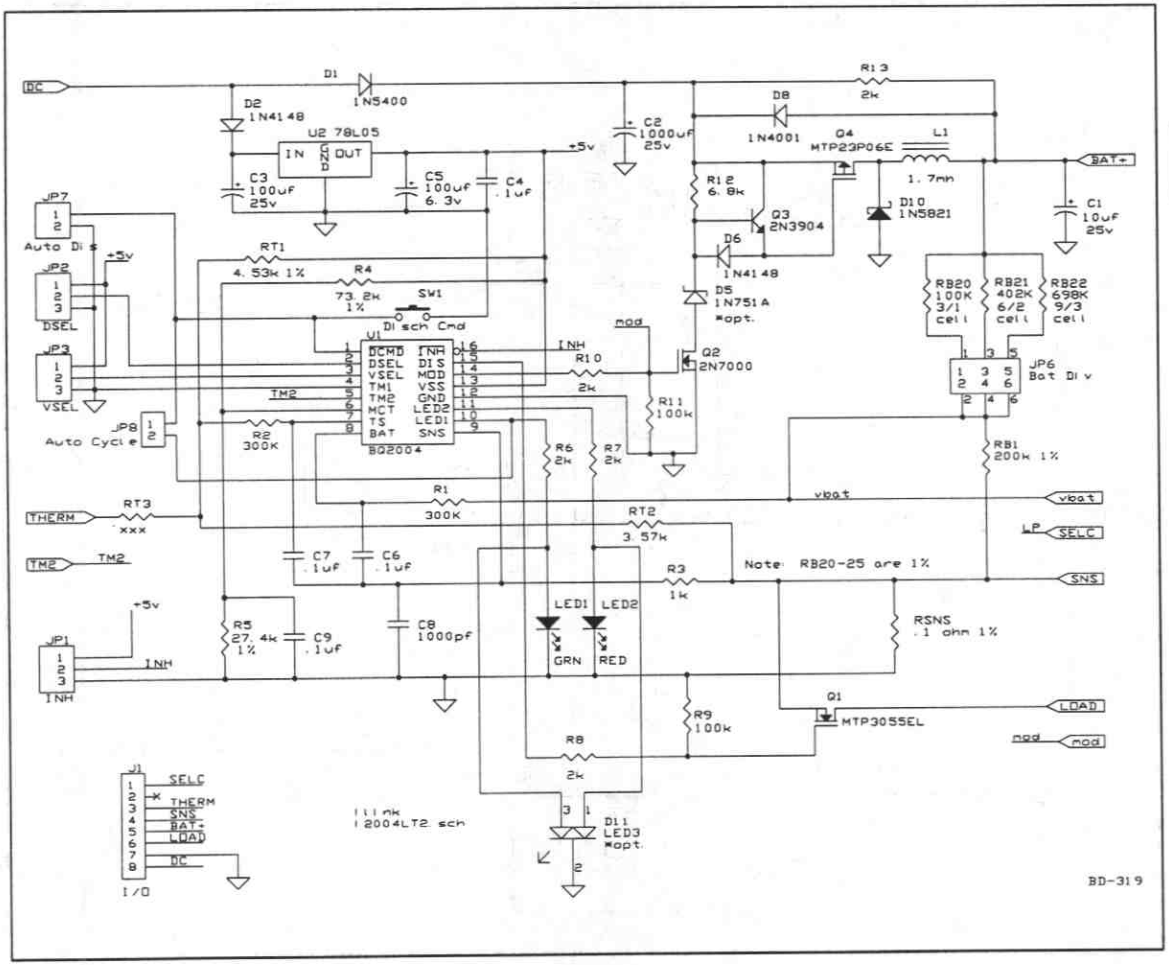
2

Recommended DC Operating Conditions

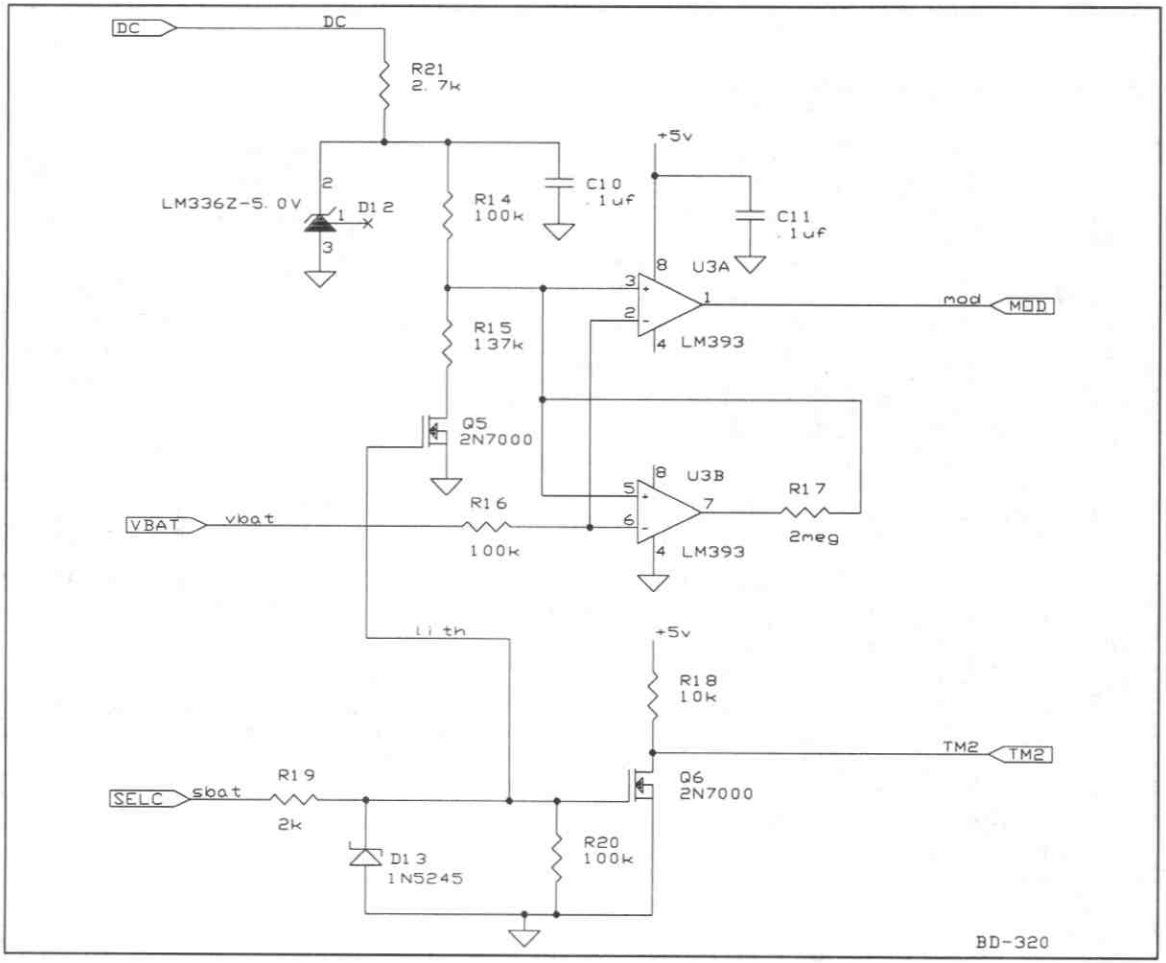
Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
I_{DC}	Maximum input current	-	-	1.5	A	
V_{DC}	Maximum input voltage	2.0 + V_{BAT} or 15	-	18 + V_{BAT} or 35	V	Note 1
V_{BAT}	BAT input voltage	-	-	24	V	
V_{THERM}	THERM input voltage	0	-	5	V	
I_{DSCHG}	Discharge load current	-	-	2	A	

Note: 1. The V_{DC+} limits consider the appropriate Zener diode at D5. The voltage at D5 is application-specific and limits the V_{GS} of Q4 to a safe enhancement value during Q4 conduction. See Table 1 for recommended D5 selections per V_{DC+}.

DV2004S3 Board Schematic



DV2004S3 Board Schematic



BENCHMARQ

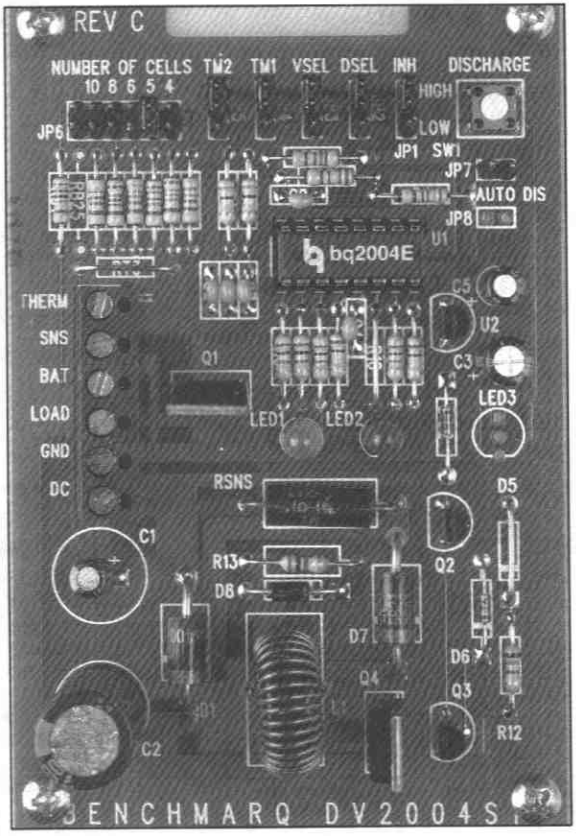
DV2004ES1

Fast Charge Development System

Control of On-Board p-FET Switch-Mode Regulator

Features

- bq2004E fast charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 3.0 A)
- Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast charge termination by delta temperature/delta time (ΔT/Δt), negative delta voltage (-ΔV) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input



General Description

The DV2004ES1 Development System provides a development environment for the bq2004E Fast Charge IC. The DV2004ES1 incorporates a bq2004E and a buck-type switch-mode regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: ΔT/Δt, -ΔV or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

The user provides a power supply and batteries. The user configures the DV2004ES1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands discharge-before-charge with push-button switch S1.

Please review the bq2004E data sheet before using the DV2004ES1 board.

Connection Descriptions

J1

THERM	Thermistor connection
SNS	Negative battery terminal and thermistor connection
BAT+	Positive battery terminal and high side of discharge load
LOAD	Low side of discharge load
GND	Ground from charger supply
DC	DC input from charger supply

JP1 $\overline{INH}$	Inhibit input
JP2 DSEL	Display select
JP3 VSEL	Voltage termination select
JP4 TM1	TM1 setting
JP5 TM2	TM2 setting
JP6 NOC	Select number of cells
JP7	Auto discharge-before-charge select
JP8	Auto cycle select

Fixed Configuration

The DV2004ES1 board has the following fixed characteristics:

V_{CC} (4.75–5.25V) is regulated on-board from the supply at connector J1 DC.

LED1 and LED2 indicate charge status.

LED3 can replace LED1 and LED2 and provide an optional tri-color LED feature.

Charge initiates on the later application of the battery or DC, which provides V_{CC} to the bq2004E.

Pin $\overline{DCMD}$ may be tied to ground through JP7 for automatic discharge-before-charge. With JP7 open, a toggle of switch S1 momentarily pulls $\overline{DCMD}$ low and initiates a discharge-before-charge. The bq2004E output activates FET Q1, allowing current to flow through an external current-limiting load between BAT+ and LOAD on connector J1.

As shipped from Benchmarq, the DV2004ES1 buck-type switch-mode regulator is configured to a charging current of 2.25A. This current level is controlled by the value of sense resistor R_{SNS} by the relationship:

$$I_{CHG} = \frac{0.225V}{R_{SNS}}$$

The value of R_{SNS} at shipment is 0.100Ω. This resistor can be changed depending on the application.

The suggested maximum I_{CHG} for the DV2004ES1 board is 3A. The maximum cell voltage (MCV) setting is 1.8V.

Zener diode D5 is used to limit Q4 V_{GS} per a given DC voltage. The board is shipped with D5 shorted. The user can modify this Zener diode for the application. Refer to Table 1 for suggested D5 values for DC voltages.

Table 1. Lookup Table for D5 Selection

+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

Note: Capacitors C2 and C3 must be changed from those shipped with the board for input voltage in excess of 24V.

With the provided NTC thermistor connected between THERM and SNS, values are: LTF = 0°C, HTF = 40°C, and TCO = 60°C. The $\Delta T/\Delta t$ settings at 30°C ($T_{\Delta T}$) are: minimum = 0.82°C/minute, typical = 1.10°C/minute.

The thermistor is identified by the serial number suffix as follows:

Identifier	Thermistor
K1	Keystone RL0703-5744-103-S1
(blank)	Philips 2322-640-63103
F1	Fenwal Type 16, 197-103LA6-A01
O1	Ozhumi 150-108-00(4)
S1	Semetic 103AT-2

Jumper-Selectable Configuration

The DV2004ES1 must be configured as described below.

$\overline{INH}$ (JP1): Enables/disables charge inhibit (see bq2004E data sheet, page 8).

Jumper Setting	Pin State
[1 2] 3	Disabled (high)
1 [2 3]	Enabled (low)

TM1 and TM2 (JP4 and JP5): Select fast charge safety time/hold-off/top-off (see bq2004E data sheet, page 7).

Jumper Setting	Pin State
[1 2] 3	High
1 [2 3]	Low
1 2 3	Float

Number of Cells (JP6): A resistor-divider network is provided to select 4 to 10 cells (the resulting resistor value equals N/2 – 1 cells). RB1 is a 150KΩ resistor, and RB2 (RB20–RB25) is jumper-selected.

Closed Jumper	Number of Cells
RB25	User-selectable
RB24	10
RB23	8
RB22	6
RB21	5
RB20	4

Temperature Disable: Connecting a 10KΩ resistor between THERM and SNS disables temperature control.

DSEL (JP2): Selects LED1 and LED2 (LED3 optional) display state (see bq2004E data sheet, Table 2, page 5).

VSEL (JP3): Selects -ΔV or peak-voltage detection, or disables voltage-based termination (see bq2004E data sheet, page 7).

AUTO DIS SELECT (JP7): Jumping JP7 enables automatic discharge-before-charge.

AUTO CYCLE SELECT (JP8): Jumping JP8 automatically initiates a continuous discharge-before-charge/fast-charge cycling for data collection purposes.

Setup Procedure

1. Configure VSEL, TM1, TM2, DSEL, $\overline{INH}$, and number-of-cells (NOC) jumpers.
2. Connect the provided thermistor or a 10KΩ resistor between THERM and SNS.
3. If using the discharge-before-charge or auto-cycle options, connect a current-limiting discharge load between BAT+ and LOAD.
4. Attach the battery pack to BAT+ and SNS. For temperature control, the thermistor must contact the cells.
5. Attach DC current source to DC (+) and GND (–) connections in J1.

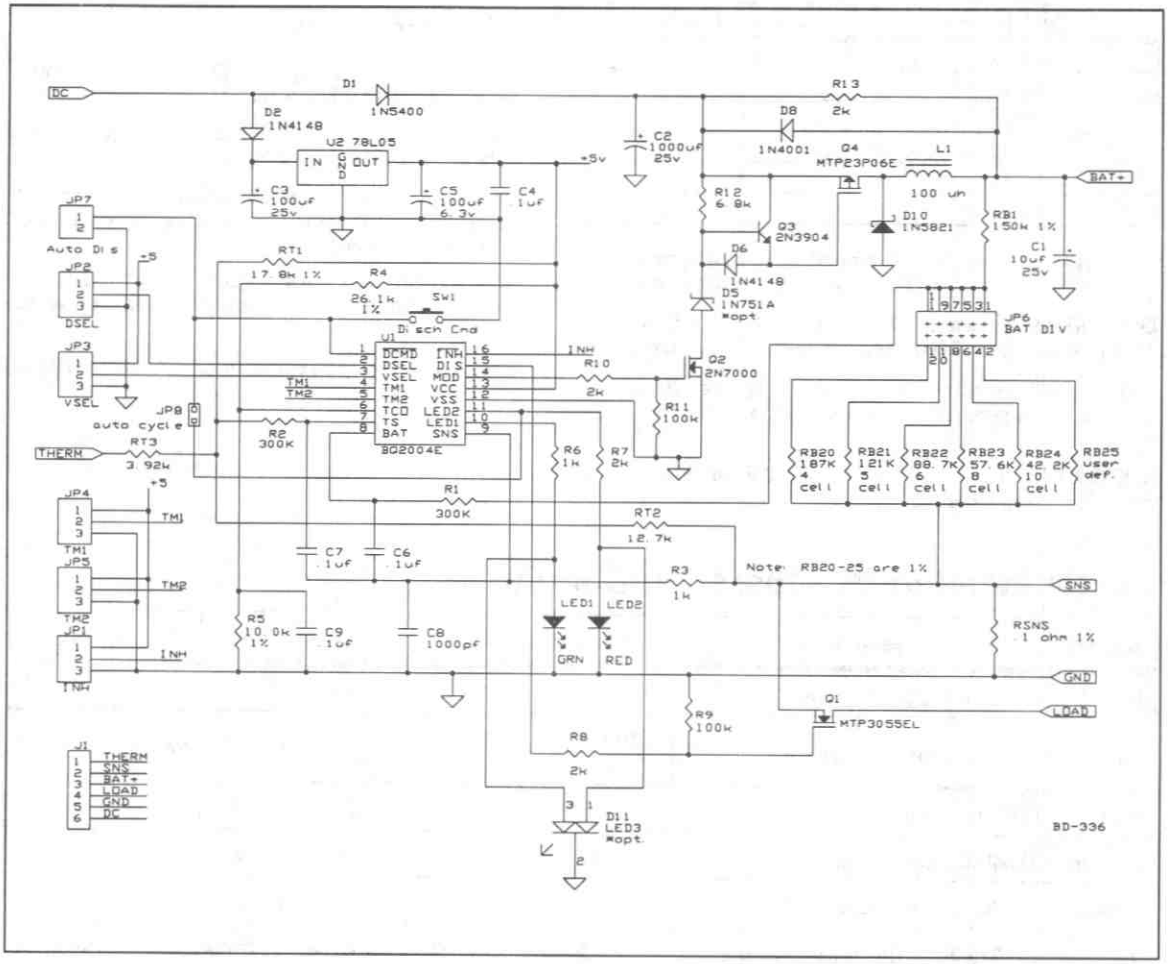
2

Recommended DC Operating Conditions

Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
I_{DC}	Maximum input current	-	-	2.4	A	
V_{DC}	Maximum input voltage	2.0 + V_{BAT} or 15	-	18 + V_{BAT} or 35	V	Note 1
V_{BAT}	BAT input voltage	-	-	24	V	
V_{THERM}	THERM input voltage	0	-	5	V	
I_{DSCHG}	Discharge load current	-	-	2	A	

Note: 1. The V_{DC+} limits consider the appropriate Zener diode at D5. The voltage at D5 is application-specific and limits the V_{GS} of Q4 to a safe enhancement value during Q4 conduction. See Table 1 for recommended D5 selections per V_{DC+}.

DV2004ES1 Board Schematic



BENCHMARQ

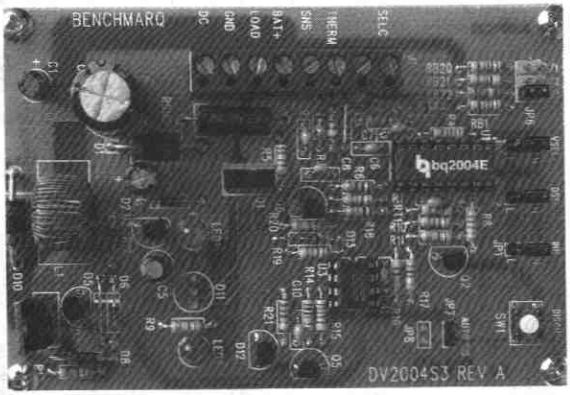
Preliminary **DV2004ES3**

Nickel/Li-Ion Development System

Control of On-Board p-FET Switch-Mode Regulator

Features

- bq2004E fast charge control evaluation and development for NiMH, NiCd and Li-Ion
- Charge current sourced from an on-board switch-mode regulator (up to 2.0 A)
- Fast charge of 3, 6, or 9 NiCd or NiMH cells and 1, 2, or 3 Li-Ion cells
- Fast charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage for nickel-based and constant-current to constant-voltage for Li-Ion
- $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input



General Description

The DV2004ES3 Development System provides a dual-chemistry development environment for the bq2004E Fast Charge IC. The DV2004ES3 incorporates a bq2004E and a buck-type switch-mode regulator to provide fast charge control for 3, 6, or 9 NiCd or NiMH cells and 1, 2, or 3 Li-Ion cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$ or peak voltage detect, maximum temperature, maximum time, maximum voltage, and inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

Fast charge for Li-Ion transitions from a constant-current to constant-voltage regulation. Voltage is regulated to within 1%. Charge complete is indicated at the maximum charge time.

The user provides a power supply and batteries. The user configures the DV2004ES3 for the number of cells and charge termination mode, and commands discharge-before-charge with push-button switch S1.

Please review the bq2004E data sheet and application note: *Applications Using Nickel-base and Li-Ion Battery Chemistries*, before using the DV2004ES3 board.

Connection Descriptions

J1

SELC	Chemistry select
THERM	Thermistor connection
SNS	Negative battery terminal and thermistor connection
BAT+	Positive battery terminal and high side of discharge load
LOAD	Low side of discharge load
GND	Ground from charger supply
DC	DC input from charger supply

Jun. 1995

1/6 Rev. A Board

JP1 $\overline{\text{INH}}$	Inhibit input
JP2 DSEL	Display select
JP3 VSEL	Voltage termination select
JP6 NOC	Select number of cells
JP7	Auto discharge-before-charge select
JP8	Auto cycle select

Fixed Configuration

The DV2004ES3 board has the following fixed characteristics:

V_{CC} (4.75–5.25V) is regulated on-board from the supply at connector J1 DC.

LED1 and LED2 indicate charge status.

LED3 can replace LED1 and LED2 and provide an optional tri-color LED feature.

Charge initiates on the later application of the battery or DC, which provides V_{CC} to the bq2004E.

Pin $\overline{\text{DCMD}}$ may be tied to ground through JP7 for automatic discharge-before-charge. With JP7 open, a toggle of switch S1 momentarily pulls $\overline{\text{DCMD}}$ low and initiates a discharge-before-charge. The bq2004E output activates FET Q1, allowing current to flow through an external current-limiting load between BAT+ and LOAD on connector J1.

As shipped from Benchmarq, the DV2004ES3 buck-type switch-mode regulator is configured to a charging current of 1.5A. This current level is controlled by the value of sense resistor R_{SNS} by the relationship:

$$I_{CHG} = \frac{0.225V}{R_{SNS}}$$

The inductor is configured for a maximum of 1.5 Amp and should not be adjusted without consulting Benchmarq.

Zener diode D5 is used to limit Q4 V_{GS} per a given DC voltage. The board is shipped with D5 shorted. The user can modify this Zener diode for the application. Refer to Table 1 for suggested D5 values for DC voltages.

With the provided NTC thermistor connected between THERM and SNS, values are: LTF = 0°C, HTF = 40°C, and TCO = 60°C. The $\Delta T/\Delta t$ settings at 30°C ($T_{\Delta T}$) are: minimum = 0.82°C/minute, typical = 1.10°C/minute.

Table 1. Lookup Table for D5 Selection

+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

Note: Capacitors C2 and C3 must be changed from those shipped with the board for input voltage in excess of 24V.

The thermistor is identified by the serial number suffix as follows:

Identifier	Thermistor
K1	Keystone RL0703-5744-103-S1
(blank)	Philips 2322-640-63103
F1	Fenwal Type 16, 197-103LA6-A01
O1	Ozhumi 150-108-00(4)
S1	Semetic 103AT-2

Jumper-Selectable Configuration

The DV2004ES3 must be configured as described below.

$\overline{\text{INH}}$ (JP1): Enables/disables charge inhibit (see bq2004E data sheet, page 8).

Jumper Setting	Pin State
[1 2] 3	Disabled (high)
1 [2 3]	Enabled (low)

Number of Cells (JP6): A resistor-divider network is provided to select 3, 6, or 9 cells (the resulting resistor value equals $N/2 - 1$ cells).

Closed Jumper	Number of Cells	
	NiCd/NiMH	Li-Ion
RB22	9	3
RB21	6	2
RB20	3	1

Temperature Disable: Connecting a 10KΩ resistor between THERM and SNS disables temperature control.

DSEL (JP2): Selects LED1 and LED2 (LED3 optional) display state (see bq2004E data sheet, Table 2, page 5).

VSEL (JP3): Selects -ΔV or peak-voltage detection, or disables voltage-based termination (see bq2004E data sheet, page 7).

AUTO DIS SELECT (JP7): Jumping JP7 enables automatic discharge-before-charge.

AUTO CYCLE SELECT (JP8): Jumping JP8 automatically initiates a continuous discharge-before-charge / fast-charge cycling for data collection purposes.

Setup Procedure

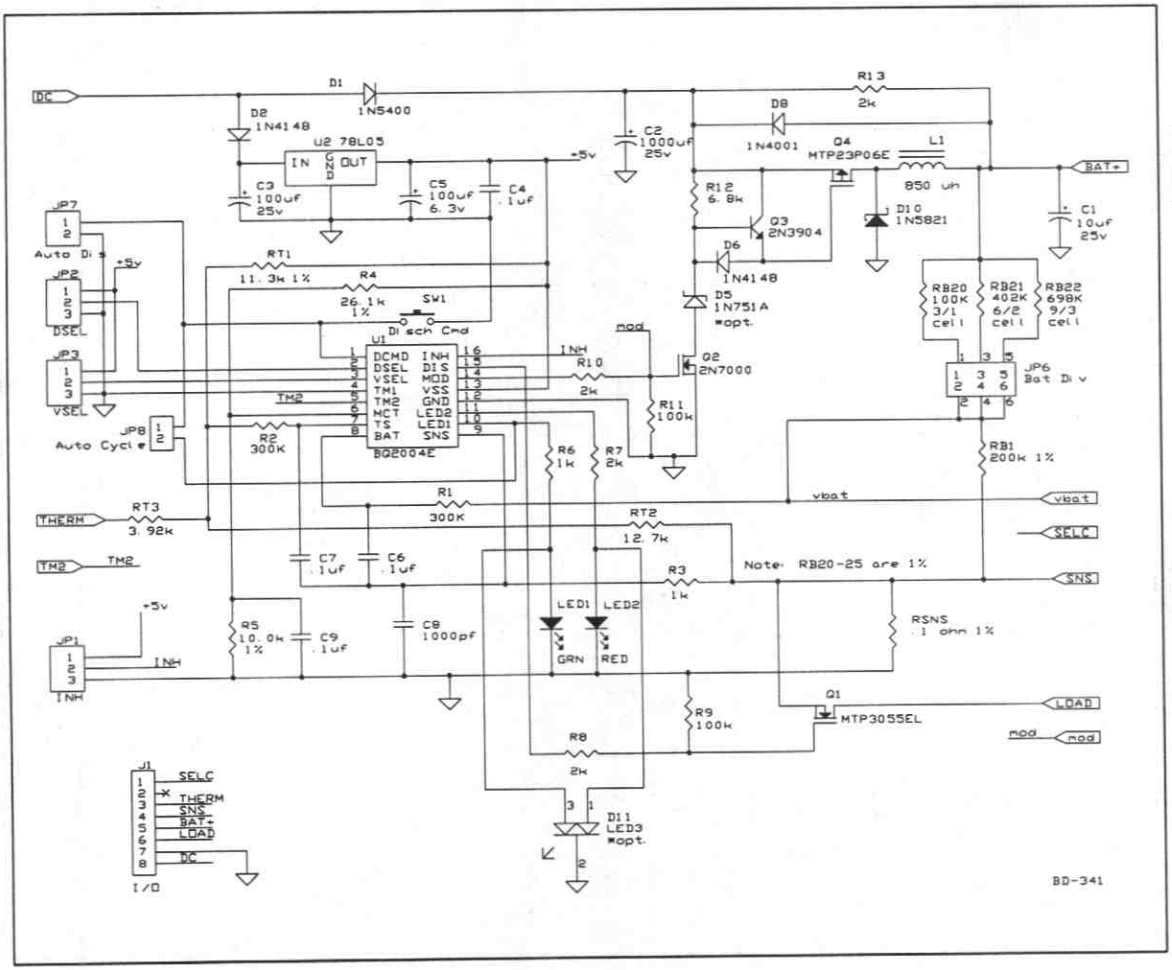
1. Configure VSEL, TM1, TM2, DSEL, $\overline{\text{INH}}$, and number-of-cells (NOC) jumpers.
2. Connect the provided thermistor or a 10KΩ resistor between THERM and SNS.
3. If using the discharge-before-charge or auto-cycle options, connect a current-limiting discharge load between BAT+ and LOAD.
4. For nickel-based battery, attach the battery pack to BAT+, SNS, and THERM. SELC should float. For Li-Ion, SELC must be connected to BAT+ to operate properly.
5. Attach DC current source to DC (+) and GND (–) connections in J1.

Recommended DC Operating Conditions

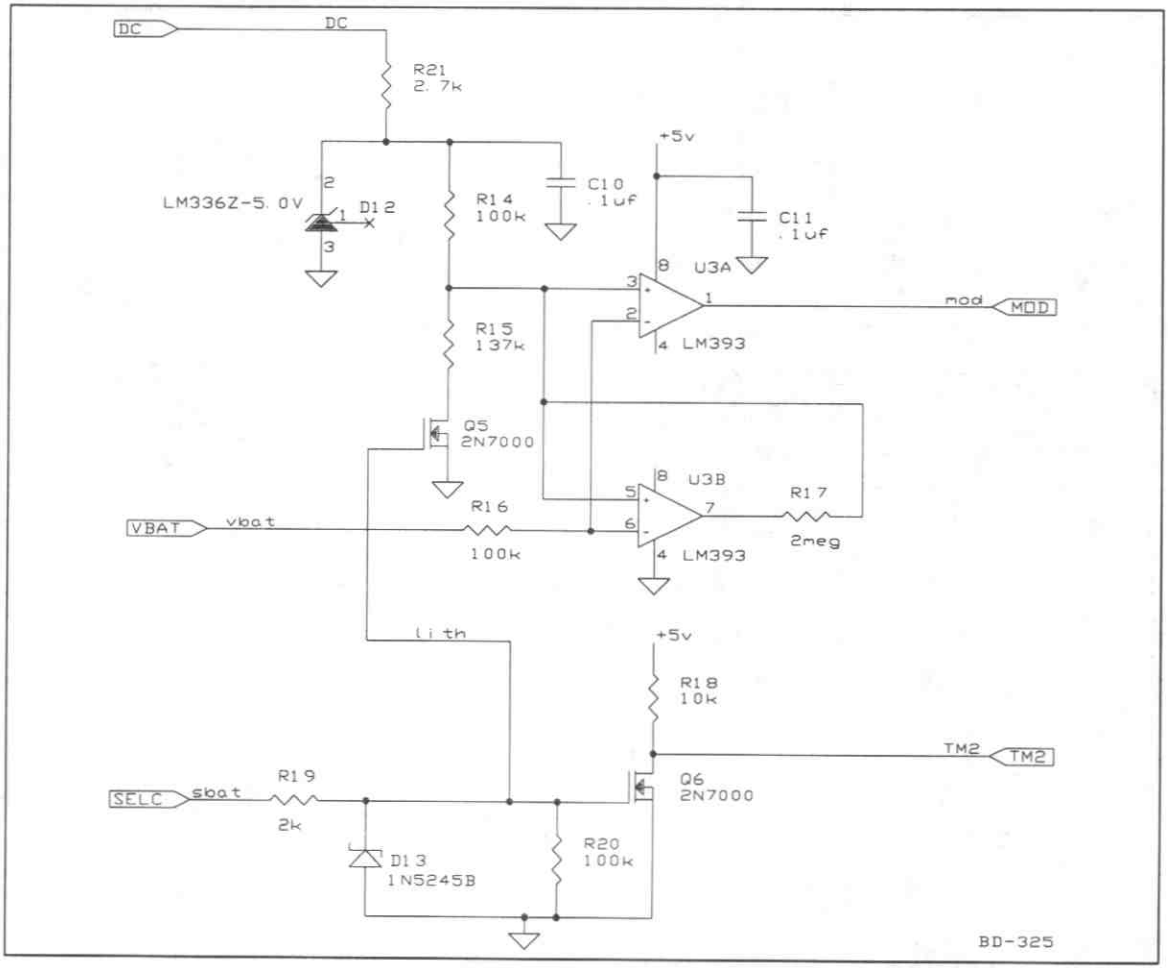
Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
I_{DC}	Maximum input current	-	-	1.5	A	
V_{DC}	Maximum input voltage	2.0 + V_{BAT} or 15	-	18 + V_{BAT} or 35	V	Note 1
V_{BAT}	BAT input voltage	-	-	24	V	
V_{THERM}	THERM input voltage	0	-	5	V	
I_{DSCHG}	Discharge load current	-	-	2	A	

Note: 1. The V_{DC+} limits consider the appropriate Zener diode at D5. The voltage at D5 is application-specific and limits the V_{GS} of Q4 to a safe enhancement value during Q4 conduction. See Table 1 for recommended D5 selections per V_{DC+}.

DV2004ES3 Board Schematic



DV204ES3 Board Schematic



Please see the *1995 Data Book* for this data sheet. The following revision history shows the Apr. 1995 revision D changes from the March 1994 revision C data sheet in the data book.

Revision D changes apply to the bq2010-D107 devices.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
3	4	EDV monitoring	Was: EDV monitoring is disabled if $V_{SR} \leq$ -150mV; Is: EDV monitoring is disabled if $V_{SR} \leq$ -250mV
3	6	Table 1, $PROG_5$	Was: $PROG_5$ = H = Reserved; Is: $PROG_5$ = H = Disable self-discharge
3	7, 8	Self-discharge	Add: or disabled as selected by $PROG_5$
3	11	Capacity inaccurate	Correction: CI is asserted on the 64th charge after the last LMD update or when the bq2010 is reset
3	13	Nominal available charge register	NACL stops counting when NACH reaches zero
3	13	Overload flag	Was: V_{SR} < -150mV Is: V_{SR} < -250mV

Note: Change 3 = Apr. 1995 D changes from Mar. 1994 C.
Changes 1 and 2; please refer to the *1995 Data Book*.

Notes

BENCHMARQ

bq2011J

Gas Gauge IC

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such as power tools with high discharge rates
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow DIP or SOIC

General Description

The bq2011J Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2011J is designed for systems such as power tools with very high discharge rates.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Initial battery capacity is set using the $PROG_{1-4}$ and SPFC pins. Actual battery capacity is automatically "learned" in the course of a discharge cycle from full to empty and may be displayed depending on the display mode.

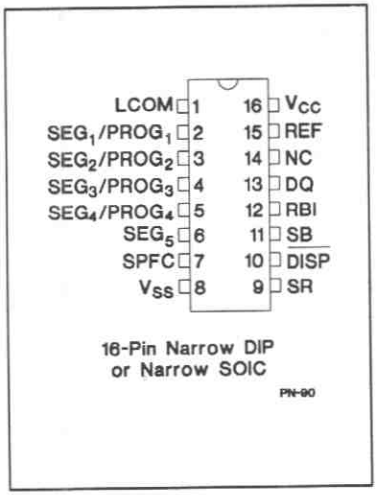
Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2011J supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2011J outputs battery information in response to external commands over the serial link. To support subassembly testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2011J gas gauge data registers.

The bq2011J may operate directly from 4 cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} from a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, and battery status.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ Program 1 input	NC	No connect
$SEG_2/PROG_2$	LED segment 2 / Program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ Program 3 input	RBI	Register backup input
$SEG_4/PROG_4$	LED segment 4/ Program 4 input	SB	Battery sense input
SEG_5	LED segment 5	$\overline{DISP}$	Display control input
SPFC	Programmed full count selection input	SR	Sense resistor input
		V_{CC}	3.0-6.5V
		V_{SS}	Negative battery terminal

Pin Descriptions

LCOM — **LED common**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of $PROG_{1-4}$ pull-up or pull-down program resistors. LCOM is high impedance when the display is off.

SEG_1-SEG_5 — **LED display segment outputs**

Each output may activate an LED to sink the current sourced from MODE, the battery, or V_{CC}.

$PROG_1$-$PROG_4$ — **Programmed full count selection inputs (dual function with SEG_1 - SEG_4)**

These three-level input pins define the programmed full count (PFC) in conjunction with SPFC pin, define the display mode and enable or disable self-discharge.

SPFC — **Programmed full count selection input**

This three-level input pin along with $PROG_{1-3}$ define the programmed full count (PFC) thresholds and scale selections described in Table 1 and Table 2. The state of the SPFC pin is only read immediately after a reset condition.

SR — **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor Rs is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor and battery pack ground (see Figure 1. $V_{SR} > V_{SS}$ indicates discharge, and $V_{SR} < V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2011J is $V_{SR} + V_{OS}$ (see Table 4 on page 8).

NC — **No connect**

$\overline{DISP}$ — **Display control input**

$\overline{DISP}$ floating allows the LED display to be active during charge and discharge if $V_{SRO} < -1mV$ (charge) or $V_{SRO} > 2mV$ (discharge). Transitioning $\overline{DISP}$ low activates the display for 4 seconds.

SB — **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) threshold and maximum cell voltage (MCV).

RBI — **Register backup input**

This input is used to provide backup potential to the bq2011J registers during periods when $V_{CC} \leq 3V$. A storage capacitor should be connected to RBI.

DQ — **Serial I/O pin**

This is an open-drain bidirectional pin.

REF — **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} — **Supply voltage input**

V_{SS} — **Ground**

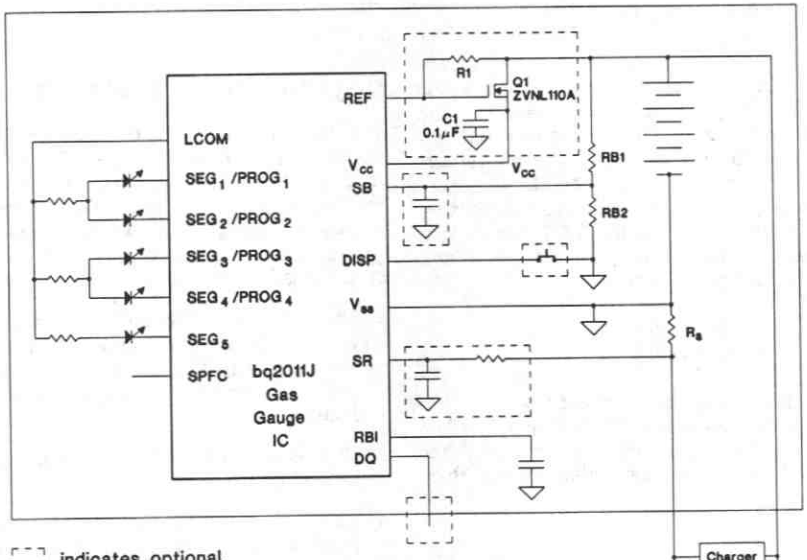
Functional Description

General Operation

The bq2011J determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011J measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011J using the LED display with absolute mode as a charge-state indicator. The bq2011J can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2011J monitors the charge and discharge currents as a voltage across a sense resistor (see Rs in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



[ ] indicates optional.

Directly connect to V_{CC} across 4 cells (4.8V nominal and should not exceed 6.5V) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of > 4 cells.

Programming resistor and ESD-protection diodes are not shown.

R-C on SR may be required (application specific), where the maximum R should not exceed 20K.

SD-308

Figure 1. Battery Pack Application Diagram—LED Display, Absolute Mode

Register Backup

The bq2011J RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2011J registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2011J checks the internal registers for data loss or corruption. If data has changed, then the NAC and FULCNT registers are cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2011J monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging. The EDV and MCV thresholds for the bq2011J are fixed at:

$$V_{EDV} = 0.90V$$
$$V_{MCV} = 2.00V$$

EDV detection is disabled if the discharge is at a rate equivalent to or greater than 6C (OVLD flag = 1) EDV detection is re-enabled approximately one second after the discharge falls below a rate equivalent to less than 6C (OVLD flag = 0).

Reset

The bq2011J recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V resets the device. Reset can also be accomplished with a command over the serial port as described on page 14.

Temperature

The bq2011J internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2011J measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2011J.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2011J. The bq2011J accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement

the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2011J adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 1. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2011J is configured for a given application by selecting a PFC value from Table 1. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) • sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.002Ω
Number of cells = 6
Capacity = 1800mAh, NiCd cells
Current range = 1A to 80A
Relative display mode
Self-discharge = C/80
Voltage drop across sense resistor = 2mV to 160mV

Therefore:

1800mAh • 0.002Ω = 3.6mVh

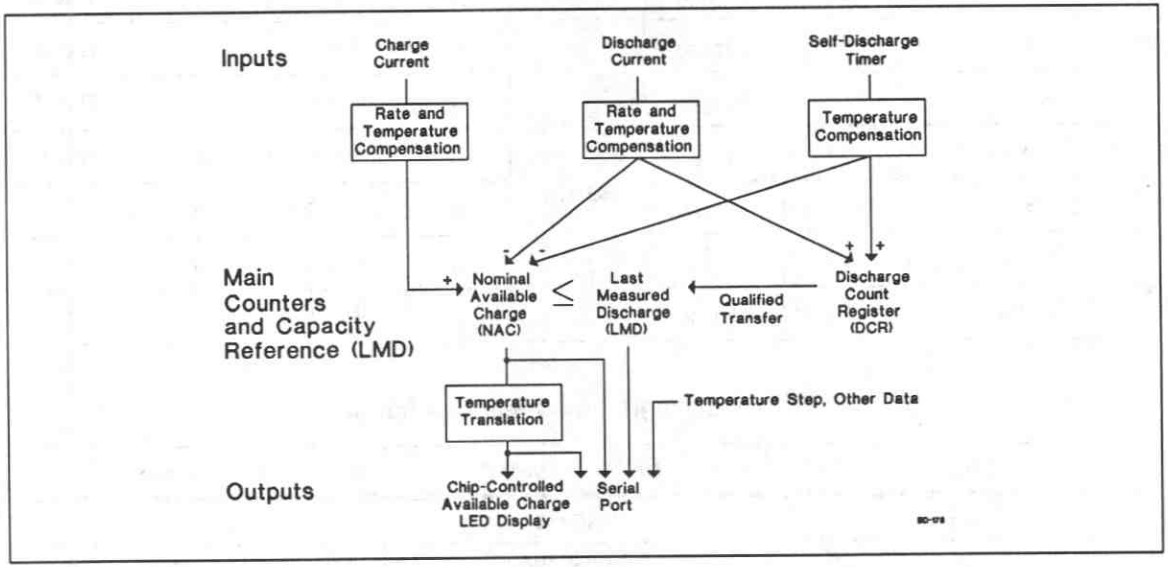


Figure 2. Operational Overview

Select:

PFC = 35840 counts or 3.39mVh
SPFC = Z (float)
PROG1, PROG2 = H or Z
PROG3 = L
PROG4 = H or Z

The initial full battery capacity is 3.39mVh (1695mAh) until the bq2011J "learns" a new capacity with a qualified discharge from full to EDV.

3. **Nominal Available Charge (NAC):**

NAC counts up during charge to a maximum value of LMD and down during discharge and self discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

Note: NAC is set to the value in LMD when $PROG_4$ is pulled low during a reset.

Table 1. bq2011J Programmed Full Count mVh Selections

Programmed Full Count (PFC)	mVh	Scale	Display Mode	SPFC	$PROG_1$	$PROG_2$	$PROG_3$
40192	3.81	1/10560	Absolute	H	H or Z	H or Z	H or Z
32256	3.05	1/10560		Z	H or Z	H or Z	H or Z
28928	2.74	1/10560		L	H or Z	H or Z	H or Z
25856	2.45	1/10560		H	L	H or Z	H or Z
35840	3.39	1/10560		Z	L	H or Z	H or Z
23296	2.21	1/10560		L	L	H or Z	H or Z
40192	3.81	1/10560	Relative	H	H or Z	L	H or Z
32256	3.05	1/10560		Z	H or Z	L	H or Z
28928	2.74	1/10560		L	H or Z	L	H or Z
25856	2.45	1/10560		H	H or Z	H or Z	L
35840	3.39	1/10560		Z	H or Z	H or Z	L
23296	2.21	1/10560		L	H or Z	H or Z	L

Table 2. Programmed Self-Discharge

$PROG_4$	NAC Reset Value	Self-Discharge
H or Z	NAC = 0	Enabled
L	NAC = PFC	Disabled

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV} if:

   - No valid charge initiations (charges greater than 256 NAC counts; or 0.006 – 0.01C) occurred during the period between NAC = LMD and EDV detected.
   - The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
   - The temperature is ≥ 0°C when the EDV level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a negative voltage on the V_{SR} input. If charge activity is detected, the bq2011J increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates an LED display if V_{SRO} < -1mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011J determines a valid charge activity sustained at a continuous rate equivalent to V_{SRO} < -400µV. A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} rises above -400µV.

Discharge Counting

All discharge counts where V_{SRO} > 500µV cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} > 2mV activates the display, if enabled. The display becomes inactive after V_{SRO} falls below 2mV.

Self-Discharge Estimation

The bq2011J continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/80 • NAC rate per day or disabled per Table 2. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot not be decremented below 0.

Count Compensations

The bq2011J determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 1). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal compensation factor. This factor is based upon the number of NAC counts per second. The actual "C" rate may be calculated by using the following formula:

$$C_{RATE} = \frac{K}{N * LMD}$$

where:

K = 66,000

N = Number of samples

LMD = Contents of address 05h

The compensations factors during discharge are:

Samples	Discharge Compensation Factor	Effective CRATE LMD = 9Dh
N > 70	1.00	C_{RATE} < 6.0C
70 ≥ N > 35	1.05	6.0C ≤ C_{RATE} < 12.0C
35 ≥ N > 23	1.15	12.0C ≤ C_{RATE} < 18.0C
N ≤ 23	1.25	C_{RATE} ≥ 18.0C

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.00 + (0.05 \cdot N)$$

Where N = number of 10°C steps below 10°C and C_{RATE} < 6.0C.

For example:

T > 10°C : Nominal compensation, N = 0

0°C < T < 10°C : N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C : N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C : N = 3 (i.e., 1.00 becomes 1.15)

-20°C < T < -30°C : N = 4 (i.e., 1.00 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of 1/80 • NAC per day or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day
< 10°C	NAC/320
10–20°C	NAC/160
20–30°C	NAC/80
30–40°C	NAC/40
40–50°C	NAC/20
50–60°C	NAC/10
60–70°C	NAC/5
> 70°C	NAC/2.5

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between -400µV and 500µV.

Table 4. bq2011J Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Communicating With the bq2011J

The bq2011J includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2011J registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011J should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends an eight-bit command byte to the bq2011J. The command directs the bq2011J to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011J may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2011J. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2011J is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2011J taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2011J to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011J is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011J NAC register.

bq2011J Registers

The bq2011J command and status registers are listed in Table 5 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2011J. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

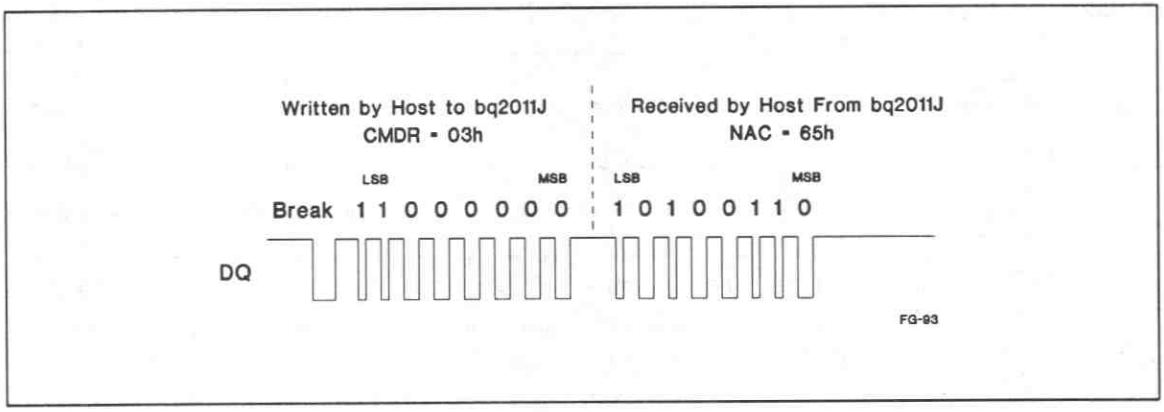


Figure 3. Typical Communication With the bq2011J

Table 5. bq2011J Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	MCV	CI	VDQ	n/u	EDV	n/u
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
OCTL	Output control register	0ah	Write	1	OC5	OC4	OC3	OC2	OC1	n/u	OCE
FULCNT	Full count register	0bh	Read	FUL7	FUL6	FUL5	FUL4	FUL3	FUL2	FUL1	FUL0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2011J outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011J flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when V_{SRO} < -400µV. A V_{SRO} of greater than- 400µV or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or V_{SRO} > -400µV

1 V_{SRO} < -400µV

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011J is reset (see the RST register description). BRP is cleared if either the bq2011J is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 bq2011J is charged until NAC = LMD or discharged until the EDV flag is asserted

1 SB rising from below 0.1V, or a serial port initiated reset has occurred

The ***maximum cell voltage*** flag (MCV) is asserted whenever the potential on the SB pin (relative to V_{SS}) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	MCV	-	-	-	-	-

Where MCV is:

0 V_{SB} < 2.0V

1 V_{SB} > 2.0V

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2011J is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2011J is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2011J is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action equal to 256 NAC counts with $V_{SRO} < -400\mu V$.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***end-of-discharge warning*** flag (EDV) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate. EDV detection is disabled if OVLD = 1. The EDV flag is latched until a valid charge has been detected.

The EDV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV	-

Where EDV is:

0 Valid charge action detected and $V_{SB} \geq 0.90V$

1 $V_{SB} < 0.90V$ providing that OVLD = 0

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2011J contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2011J calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 • NAC / "Full Reference"
< -20°C	0.5 • NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011J. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

If SEG_5 = 0 on reset, then NACH = PFC and NACL = 0. If SEG_5 = Z or H, the NACH and NACL registers are cleared to zero, NACL stops counting when NACL reaches zero. When the bq2011J detects a valid charge, NACL resets to zero; *writing to the NAC register affects the available charge counts and, therefore, affects the bq2011J gas gauge operation.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2011J. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011J uses as a measured full reference. The bq2011J adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011J updates the capacity of the battery. LMD is set to PFC during a bq2011J reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011J flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the present discharge regime as follows:

DR2	DR1	DR0	C_{RATE}@LMD = 90h
0	0	0	C_{RATE} < 6C
0	0	1	6C ≤ C_{RATE} < 12C
0	1	0	12C ≤ C_{RATE} < 18C
0	1	1	C_{RATE} ≥ 18C

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, C_{RATE} ≥ 6.0C for LMD = 90h (see Discharge Compensation, page 8). OVLD remains asserted as long as the condition is valid.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Full Count Register (FULCNT)

The read-only FULCNT register (address=0bh) provides the system with a diagnostic of the number of times the battery has been fully charged (NAC = LMD). The number of full occurrences can be determined by multiplying the value in the FULCNT register by 16. Any discharge

action other than self-discharge allows detection of another full occurrence during the next valid charge action.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2011J adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. The register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. CPI is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011J. The segment drivers may be overwritten by data from OCTL when the least-significant bit of OCTL, OCE, is set. The data in bits OC_{5-1} of the OCTL register (see Table 5 on page 10 for details) is output onto the segment pins, SEG_{5-1}, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2011J to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2011J as explained below. Note: Whenever the OCTL register is written, the MSB of OCTL should be written to a logic one.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. A full device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed,*** *and results in improper operation of the bq2011J.*

Resetting the bq2011J sets the following:

- LMD = PFC
- CPI, VDQ, OCE, and NAC = 0
  (NAC = PFC when $PROG_4$ = L)
- CI and BRP = 1

Display

The bq2011J can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to V_{CC}, the battery, or the MODE pin for programming the bq2011J.

The bq2011J displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description on page 12.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} < -1mV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} > 2mV. When pulled low, the segment output becomes active for 4 seconds, ±0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV} to indicate a low-battery condition or NAC is less than 10% of the LMD or PFC, depending on the display mode.

Microregulator

The bq2011J can operate directly from 4 cells. To facilitate the power supply requirements of the bq2011J, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2011J can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011J application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.87	0.90	0.93	V	SB
V_{SRQ}	Valid charge	-	-	-400	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	500	-	-	µV	$V_{SR} + V_{OS}$
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB

Note: For proper operation of the threshold detection circuit, V_{CC} must be at least 1.5V greater than the voltage being measured.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data-retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} > V_{SS} = discharge; V_{SR} < V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IHPFC}	PROG/SPFC logic input high	V_{CC} - 0.2	-	-	V	SPFC, $PROG_{1-4}$
V_{ILPFC}	PROG/SPFC logic input low	-	-	V_{SS} + 0.2	V	SPFC, $PROG_{1-4}$
V_{IZPFC}	PROG/SPFC logic input Z	float	-	float	V	SPFC, $PROG_{1-4}$
I_{IHPFC}	PROG/SPFC input high current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
I_{ILPFC}	PROG/SPFC input low current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCOM} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At V_{OL} = V_{SS} + 0.3V, DQ
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	SPFC, $PROG_{1-4}$

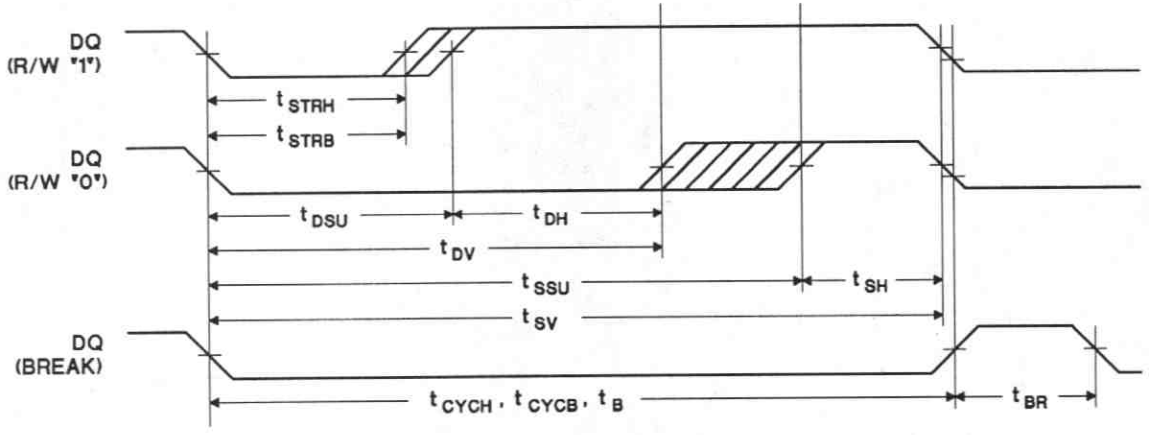
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2011J	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2011J to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2011J	5	-	-	ns	
t_{STRB}	Start hold, bq2011J to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

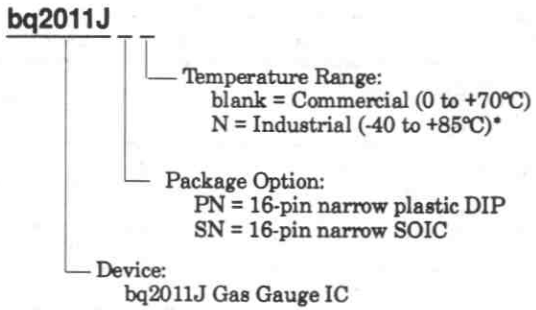
Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



RC-34

Ordering Information



* Contact factory for availability.

BENCHMARQ

EV2014

Gas Gauge Evaluation Board

Contents

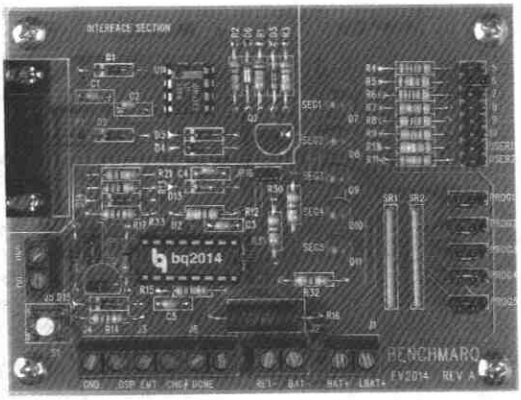
Introduction

The bq2014 Gas Gauge IC provides battery capacity monitoring in a single 16-pin SOIC or DIP package. The EV2014 Evaluation Board provides a useful means to test bq2014 functionality and easily interface with the device over the RS-232 port of a PC. The bq2014 features:

- Battery capacity monitoring functions
- LED display of available charge
- DQ serial I/O port communications functions

Functional Description

The EV2014 provides functional evaluation of the bq2014 IC on a PCB. The actual implementation of a bq2014-based design will be significantly smaller in size. See the bq2014 data sheet (Dec. 1994 B or later) for bq2014 specifications.



Power Source

The bq2014 derives its Vcc from either an external source or from the battery connected to the BAT+ (J1) and BAT– (J2) terminal blocks. Refer to Table 4 in *Using the bq2010—A Tutorial for Gas Gauging* for the proper size of R17 as part of the Vcc regulation. The EV2014 Evaluation Board is shipped with a 200KΩ resistor for R17.

Current Path

The bq2014 uses a sense resistor (R16) on the negative terminal of the battery to measure charge and discharge of the battery. This resistor may be changed if necessary. The system load is connected between the BAT+ (J1) and RET– (J2) terminal blocks (see the schematic in Appendix C).

Parameter Programming

The EV2014 is programmed by the segment programming pins, using jumpers PROG1–PROG6. The programming pins determine:

- Programmed full count
- Scale factor
- Self-discharge rate
- Display mode

EV2014 Contents

Each package contains the following items:

1 EV2014 PC Board

This includes the bq2014 sample, current regulator, programming jumpers, battery divider resistors, and the PC serial port interface.

1 EV2014 DQ/RS-232 Cable

1 EV2014 (v2.0) User Interface Program Diskette

This program runs on *any AT-compatible computer* equipped with a standard RS-232 (COM1, COM2, COM3, or COM4) serial port, and provides the user with a complete menu-driven system to control, monitor, and log data from the EV2014 Evaluation Board. The User Interface Program communicates with the bq2014 over the DQ serial I/O port using the RS-232 interface.

Please check to make sure that all items are present and in good condition. If you have any problems, please contact your Benchmarq representative or call Benchmarq.

EV2014 Connections

The connections for the EV2014 are described below. Please refer to the attached schematic in conjunction with these descriptions.

JP1–JP8 Battery cell divider. JP1-JP6 are used to divide the battery voltage by 5 to 10. JP7 and JP8 are user-definable, but are configured for 11 and 12 cells on this board.

JP9 **V_{CC} supply.** This jumper is used to select the V_{CC} supply for the bq2014. When JP9 is near Q2, the supply is taken from the BAT+ input and is regulated by the bq2014 and Q2. When JP9 is near R13, the V_{CC} supply is provided by LBAT+. If V_{CC} is supplied by LBAT+, it must not exceed the specified V_{CC} voltage range in the bq2014 data sheet (Dec. 1994 B or later).

JP10–JP14 Programming pins 1–5. These jumpers are used to configure the programming pins. When the jumper is positioned near the PROG# designator, the pins are pulled high. If the jumper is in the other position, the pins are pulled low. If the jumper is removed, the pins are in the high-impedance state. The board is shipped with all pins in the high position. Please refer to the bq2014 data sheet (Dec. 1994 B or later) for the proper configuration of $PROG_{1-5}$.

JP16 LED enable (LCOM connection). This jumper connects the LCOM pin of the bq2014 to the LEDs. The board is shipped with this jumper enabled.

EMPTY EMPTY output. This connection allows the user to monitor the EMPTY output pin provided on the bq2014. This pin is high-impedance when the single-cell divided battery voltage is less than the EDVF threshold (final end-of-discharge warning).

DSP Display input ($\overline{DISP}$ pin). DSP is connected in parallel with the push-button switch S1 provided on the EV2014 board. An external switch configuration can be made using DSP. When the EV2014 is floating and detects charging or discharging, the LED outputs are active to reflect the charge state. When the $\overline{DISP}$ input is pulled low, the LEDs reflects the charge state.

EV2014 Configuration

The EV2014 Evaluation Board may be used with or without the DQ/RS-232 Interface Program. The Evaluation Board should first be configured before connecting the battery or the RS-232 cable.

Step 1 Enabling the LEDs (optional)

JP16 should be installed.

Step 2 Connecting the power supply

The EV2014 can operate from power provided by the battery being monitored or from LBAT+. Set the battery divider (JP1–JP8) to the correct number of battery cells prior to connecting the battery. If the bq2014 will be powered from the battery, connect JP9 closer to Q2. If the bq2014 will be powered from an external supply, connect JP9 closer to R13. **Important: Connect the battery ONLY after setting JP1-JP8 and JP9.**

Step 3 Connecting the RS-232 cable

Connect the cable provided to the serial port of any PC. Please ensure no memory-resident programs use this serial port.

Step 4 Connecting the load

The external load is connected between BAT+ and RET- (J2) on the EV2014. A

sense resistor (R16) is in series with the negative terminal of the battery. The EV2014 board is supplied with a 0.1, 1% 3W resistor. Please ensure that the discharge load does not exceed the V_{SR} specification for the bq2014. R16 may be changed to a different-value resistor.

Installing the User Interface Program

The User Interface Program (named "EV2014") runs on any PC-compatible computer. The program may be run from the disk provided, or it may be installed on any directory on the computer's hard disk. To run the program from the hard disk, simply copy all the files from the disk supplied to the hard disk. All the files should reside in the same directory.

The User Interface Program installs a driver to control the DQ/RS-232 interface. This driver asks which COM port is connected to the EV2014 Evaluation board. If communication is not established with the EV2014 board, the Main Menu does not appear. Please refer to Appendix B (Troubleshooting) if the program does not establish communication with the EV2014.

The EV2014 uses the PC-AT real-time clock to provide the proper bit timing for serial communication with the bq2014. The modem control lines are used as the single-wire serial interface to the bq2014. Any TSR that uses the PC real-time clock affects the operation of the EV2014. For proper operation, the EV2014 should not be operated from a DOS shell program.

If the PC is a notebook or portable type, it may be configured to save battery power by adjusting the clocks according to the activity under way. Configure the notebook to run in "High Performance" mode for reliable communication between the EV2014 and the PC. The EV2014 UIP terminates if communication with the EV2014 board is lost.

Start the User Interface Program as follows:

```
C>EV2014
```

Using the EV2014 Program

EV2014 is a menu-driven program. Almost all of the functions and entries are made by positioning the highlighted cursor on the function desired and pressing the ENTER key, or by typing a value and then pressing the ENTER key.

Key functions are as follows:

ARROW keys	Use the arrow keys to move the highlighted cursor around the screen.
ENTER key	Press the ENTER key to select the value currently being displayed for a parameter, or to perform a function selected by the highlighted cursor.
ESCAPE key	Press the ESCAPE key to escape from any function back to the main menu, or to escape from any parameter value screen back to the menu displaying that parameter.
F3 key	Press the F3 key to display a help file for the selected function or parameter.

Main Menu

The Main Menu appears after the EV2014 program has started. If this menu does not appear, communication with the EV2014 has not been established; please refer to Appendix B (Troubleshooting) if the EV2014 does not display the Main Menu.

The Main Menu shows six functions that may be activated; see Figure 1. Use the cursor keys (arrow keys) to position the highlighted cursor over the function to be activated and press the ENTER key. For help, press the F3 key, and a help note about the function appears. Press the ESCAPE key to exit from the EV2014 program.

The Main Menu functions are as follows:

<Initialize>	Sends a reset command to the bq2014.
<Monitor>	Activates a screen from which the bq2014 activity is monitored on a real-time basis.
<Digital Filter>	Activates a screen from which the Digital Magnitude Filter can be changed. The default filter value is -0.3mV, +0.38mV. The bq2014 data sheet (Dec. 1994 B or later) defines valid options for this filter.
<Data Log>	Allows entering a file name to which bq2014 data will be logged, and the logging period in seconds. When the log is activated, the display changes to the Monitor screen with a top display of: Logging Record: xx
<Display Program Menu>	Activates a screen showing the current program settings for the bq2014.
<Measure V_{OS}>	This allows the user to determine the apparent offset voltage of the bq2014 under test. A minimum of 6 minutes are required to complete the V_{OS} measurement, which has a resolution of ±0.15mV per 6 minutes.

Monitor Screen

This screen monitors real-time changes of the bq2014; see Figure 2. The program continually updates the monitor screen. As conditions change, the new values are displayed.

Time	Time of day in HH:MM:DD, 24-hour notation.
Empty/Full	This indicates the current value for GG in the TMPGG register of the bq2014. The capacity value is given in 1/16th steps.
Date	Current date in MM/DD/YY notation.
NAC	NAC register values multiplied by the scale value and divided by the sense resistor value to give mAh.
LMD	Last Measured Discharge expressed in terms of mAH. This is the 8-bit LMD register value multiplied by the scale value times 256 and divided by the sense resistor to give mAh.
Sense Resistor Value	This is the sense resistor value from the Programming menu.
Average V_{SR} Current	This is the average battery current.
Time Remaining	During discharge only, this is the time remaining at the average current (NAC / Avg. V_{SR} current)
Digital Filter Setting	This is the value of the digital magnitude filter.
Temp Step	This is a display of the active temperature step, which ranges from 0 (for temperatures <-30°C) to 12 for temperatures > 80°C).
Activity	This indicates the charging/discharging activity occurring with the battery. CHARGE is displayed if the battery is charging, while DISCHARGING is displayed if the battery is being discharged, or if it is idle (no charging taking place). OVERLOAD is displayed if the voltage drop across the sense resistor exceeds the V_{SR1} threshold. Please note that the appearance of CHARGE or DISCHARGE indicators is rate-dependent, and may take some time after the application of a charging current or a discharge load depending on the PFC and scale selected, and the rate of charge or discharge being applied.
VSR Step	This is the value of the V_{SR} current step as defined in the bq2014 data sheet.
GG Step	This is the lower four bits of the TMPGG register that correspond to the current NAC value relative to either the LMD or the original programmed full count (as determined by $PROG_{1-4}$). The GG step is reported as a step number from 0 to 15, with step 0 representing available capacity from 0 to 1/16 of full, and 15 representing available capacity from 15/16 full to full.
Charge Rate	Indicates whether the present charge is TRICKLE or FAST depending on the state of the charge rate (CR) bit in FLGS2.

```
        Benchmarq BQ2014 Evaluation Board Main Menu (v2.3)

              <Initialize>                <Monitor>

              <Digital Filter>            <Data Log>

              <Display Program>           <Measure Vos>


      Please enter the SR, # of cells in Display Program for Proper Operation


                        ESC to exit program     F3 for Help
```

Figure 1. Main Menu

First EDV This is the state of the EDV1 flag as programmed in the Display Program Menu. The default is 1.05V. The EDV1 flag latches ON if V_{SB} drops below the EDV1 threshold value. It remains latched until charging is detected, at which time it is cleared.

Cell voltage This is the cell voltage at the SB pin of the bq2014.

Battery voltage This multiplies the cell voltage by the number of cells programmed in the Display Program Menu. The default is one cell.

Battery Removed This is the state of the battery removed flag. It is set (BRM = yes) if one of the conditions indicating battery removed occurs. This flag is reset when the battery is replaced.

Valid Discharge This is the state of the VDQ bit in FLGS1. VDQ = yes if the bq2014 is charged until NAC = LMD. VDQ = no indicates the present discharge is not valid for LMD update.

Final EDV This is the state of the EDVF flag as programmed in the Display Program Menu. The value of EDVF is 0.1V lower than EDV1. The EDVF flag latches ON if V_{SB} drops below the EDVF threshold value. It remains latched until charging is detected, at which time it is cleared.

Battery Replaced This is the state of the battery replaced flag. It is set (BRP = yes) if the battery valid condition returns after setting the battery removed flag. The battery replaced flag is cleared if the battery is discharged to the EDV1 level or if it is charged to NAC = LMD. This flag is set after a EV2014 initialization.

```
Benchmarq BQ2014 Evaluation Board Real-Time Monitor Screen

    Time: 99:99:99        EMPTY ****_____FULL       Date: 99-99-9999

    NAC: 99999 mAH        LMD:  99999 mAH   Sense Resistor Value: XXXmΩ

    Avg Vsr Current: ±9999mA                Time remaining: 9999 min.

    Digital Filter Setting:  -0.XXmV=Vsrd  +0.XXmV=Vsrq    Temp Step:  XX

    Activity: XXXXX    Vsr Current Step:  XX          GG Step: XX

    Charge Rate: XXXX       First EDV:  XXX             Batt. Rem'vd: XXX

    Valid Discharge: XXX    Final EDV:  XXX             Batt. Repl'd: XXX

    Cell Voltage: XXX V     Batt. Voltage: XXX V

    Capacity Inaccurate: XXX   Capacity Inaccurate Count: XXX

FLGS1: X X X X X _ X X              FLGS2: X X X X _ _ _ X
       C B B C V N E E                     C D D D N N N O
       H R R I D / D D                     R R R R / / / V
       G P M   Q U V V                       2 1 0 U U U L
       S         1 F                                   D

   ESC to main menu       F1 to modify NAC       F2 to modify LMD
```

Figure 2. Real-Time Monitor Screen

Capacity Inaccurate	This is the state of the capacity inaccurate bit in FLGS1. It is set (CI = yes) to indicate that the battery capacity has not been updated during the last 64 charge cycles.
Capacity Inaccurate Count	This is the number of charge cycles between an LMD update. This counter is reset to zero when NAC = LMD after a valid LMD update.
FLGS1	This indicates the present state of the FLGS1 resistor.
FLGS2	This indicates the present state of the FLGS2 resistor.

Digital Magnitude Filter Menu

This menu sets the digital magnitude filter in the bq2014; see Figure 3. Any value from 1 to 255 is valid. Suggested values are displayed on the menu.

Modifying NAC and LMD

It is possible to change the values of the NAC and LMD parameters from the screen using the F1 and F2 function keys as follows.

Changing NAC (F1)

1) Press the F1 key. The NAC field is highlighted.
2) Enter the value in mAH and press the ENTER key to store the value.

Note: Changing NAC disqualifies a subsequent LMD update.

Changing LMD (F2)

1) Press the F2 key. The LMD field is highlighted.
2) Enter the value in mAH and press the ENTER key to store the value.

Data Logging

The data log is activated from the Main Menu by selecting the Data Log function. A filename to be used and the log sample period must be entered. For example:

Log Data to Filename: <filename.ext>
Enter Sample Period (10 sec or greater):<xx>
Opening Data Log File

When the data log is started, the Monitor Screen displays the number of the current log record between the time and date fields at the top of the screen. To terminate the data log, press the ESCAPE key. The file is closed and data logging is terminated.

The data log record contains fields of ASCII data separated by tab characters. The field names and descriptions in record order are listed below.

TIME	Time record written in seconds
LMD	LMD value in mAh
NAC	NAC value in mAh

```
Benchmarq BQ2014 Evaluation Board Digital Magnitude Filter Menu

Enter DMF Value from List below:  XXX

   Current Setting   -0.XXmV=Vsrd      +0.XXmV=Vsrq
   Current Threshold (DMF(mv)/Rsns): XXXXmA
   Suggested DMF Settings:          DMF   Vsrd(mV)   Vsrq(mV)
                                     75     -0.60       0.75
                                    100     -0.45       0.56
                                   *150     -0.30       0.38
                                    175     -0.26       0.32
                                    200     -0.23       0.28
            * = Default Value

                ESC to main menu      F1 to modify DMF
```

Figure 3. Digital Magnitude Filter Menu

Avg. Discharge Current	Average V_{SR} battery current
BATV	Battery cell voltage
FLAGS1	Binary setting of FLAGS1 flags:

Bit	Meaning
0	EDVF flag state
1	EDV1 flag state
2	Not used
3	VDQ (valid discharge)
4	Capacity inaccurate
5	Battery removed flag state
6	Battery replaced flag state
7	Charge active flag state

FLAGS2 Binary setting of FLAGS2 flags:

Bit	Meaning
0	Overload flag state
1–3	Not used
4–6	Discharge rate
7	Charge rate

The log records should be readable by most spreadsheet programs.

Display Program Menu

This menu is accessed by selecting the <Display Program> function on the Main Menu. The programming menu allows the user to set and observe the program state of the bq2014; see Figure 4. To change the bq2014 PFC programming, reconfigure jumpers JP10–JP14 and initialize the bq2014. The reset allows the bq2014 to read the program pins.

Sense Resistor Press F1 to enter the value of sense resistor in ohms. Typical values range from 0.02 to 0.1Ω.

The sense resistor value is used by the EV2014 UIP to develop meaningful information in terms of A, mA, and mAH in relation to battery capacity and current. The default value is 0.1. Values from 0.005 to 0.256 are saved in the battery ID RAM byte of the bq2014. Values greater than 0.256 must be re-entered each time EV2014 is started.

Scale Factor Select the scale factor from the available scales using JP12.

Like the sense resistor, the scale factor is used to develop meaningful information for the programmed full count tables, battery full, and available capacity indications.

```
                Benchmarq BQ2014  Programming Menu

Sense Resistor:      0.1 Ω          Scale Factor:      1/320

Display Full:        RELATIVE       PFC  Count: XXXXX
                                    PFC(mVH):   XXXX

Self-Discharge                      Battery Capacity   9999 mAH
Rate:                1/47 NAC/day
Number of Cells: X
EDV1:                X.XX
Programming Pin Configuration
  Prog-1  *    Prog-4  *
  Prog-2  *    Prog-5  *
  Prog-3  *    Prog-6  *

          F1 = SR, F2 = NOC, F3 = EDV1, ESC to main menu
```

Figure 4. Display Program Menu

Display Full	Use JP15 to choose between RELATIVE and ABSOLUTE full reference for the LED display.
PFC Count	Program full count from Table 2 from the bq2014 data sheet.
PFC	Select the programmed full count using JP10 and JP11. Note that the selected PFC and the sense resistor value are used to determine the initial battery full capacity (mAh) represented by the PFC.
Battery Capacity	This display indicates the battery capacity represented by dividing the PFC by the sense resistor. In practice, picking a PFC and sense resistor that provide a battery full value slightly lower than (within 5%) the rated battery capacity is recommended.
Self-Discharge Rate	Select one of two available self-discharge rates depending on the application and battery type using JP13.
Number of Cells	Press F2 to enter the number of cells in the battery stack. This shows the battery pack voltage on the monitor screen.
EDV1	Press F3 to enter the desired end of discharge voltage for the battery pack. The default value is 1.05V for the bq2014.
Programming Pin Configuration	This displays indicates the programming of the bq2014 by displaying H, Z, or L depending on the state of the program pins. Please refer to the bq2014 data sheet for further details.

Measure V_{OS} Screen

This screen is used to measure the V_{OS} of the bq2014; see Figure 5. A minimum of 360 seconds are required to perform this test. Pressing the ESC key terminates the test in progress. Operating the test for a longer period increases the resolution of the test. A "beep" signals test completion.

```
                Benchmarq EV2014 Evaluation Board Vos Measurement

          Present DMF Setting          -XXXmV=Vsrd      +XXXmV=Vsrq
          Current Threshold (DMF(mv)/Rsns): XXXXmA
          Do you want to test Vos?:  Y/N
          Calculated Vos:  Vos  XXXmV, over last xxxx seconds
          Elapsed time:  XXXX seconds



     **Note:  There must be no charge/discharge activity on the bq2014 for this test
              to be valid.  Running the test for a longer period of time increases
              the Vos measurement resolution.  This test requires a minimum
              of 6 minutes before any value is displayed.

                ESC to main menu
```

Figure 5. V_{OS} Measurement Screen

Appendix A: AP14A User's Guide

The AP14 utility (AP14A.EXE) is used to communicate with the bq2014 on a register basis. AP14 uses a driver to communicate with the EV2014 over serial port on a PC-AT personal computer.

AP14

The AP14 utility is started by executing AP14A.EXE. After AP14 is started, the following prompt is displayed:

Select COM Port < 1 2 3 4 >

Commands

The user can respond with various commands at the prompt. Pressing "Q" causes the program to terminate.

-> ?

Pressing the ? key displays following menu:

```
The following commands are available:
    ?          This display is shown.
    A          Send break.
    Q          Quit and return to DOS.
    R#         Read at address #.
    S#         Scan at address #.
    W# = **    Write at address # value **.
```

These commands may be used to send or receive data from the EV2014.

-> A

If A is entered in response to ->, then a break bit is sent to the EV2014. This may be used to restart the communication if a problem appears. If the prompt does not return immediately, then proper communication has not been established; please refer to Appendix B for troubleshooting procedures.

-> R#

If R# is entered in response to ->, where # is an applicable address in HEX format, AP14 returns the value at that location from the EV2014. The addresses are defined in the bq2014 data sheet. For example:

-> R03

causes the display to show:

R03= ##

where ## is the current NAC value in HEX format.

Address 00 is used to read and display all readable registers.

-> S#

If S# is entered in response to ->, where # is a valid bq2014 address in HEX format, AP14 continuously reads and displays the value at that location. The addressed are defined in the bq2014 data sheet. For example:

-> S03

causes the display to show:

Address 3 = ## after XXX.XX sec.

where ## is the value at location 03 and XXX.XX is the number of seconds between changes in this value.

-> W# = **

If W#=** is entered in response to ->, where # is an applicable address in HEX format and ** is the value to be written, AP14 writes the value to that location. The addresses are defined in the bq2014 data sheet. For example:

-> W05 = A0

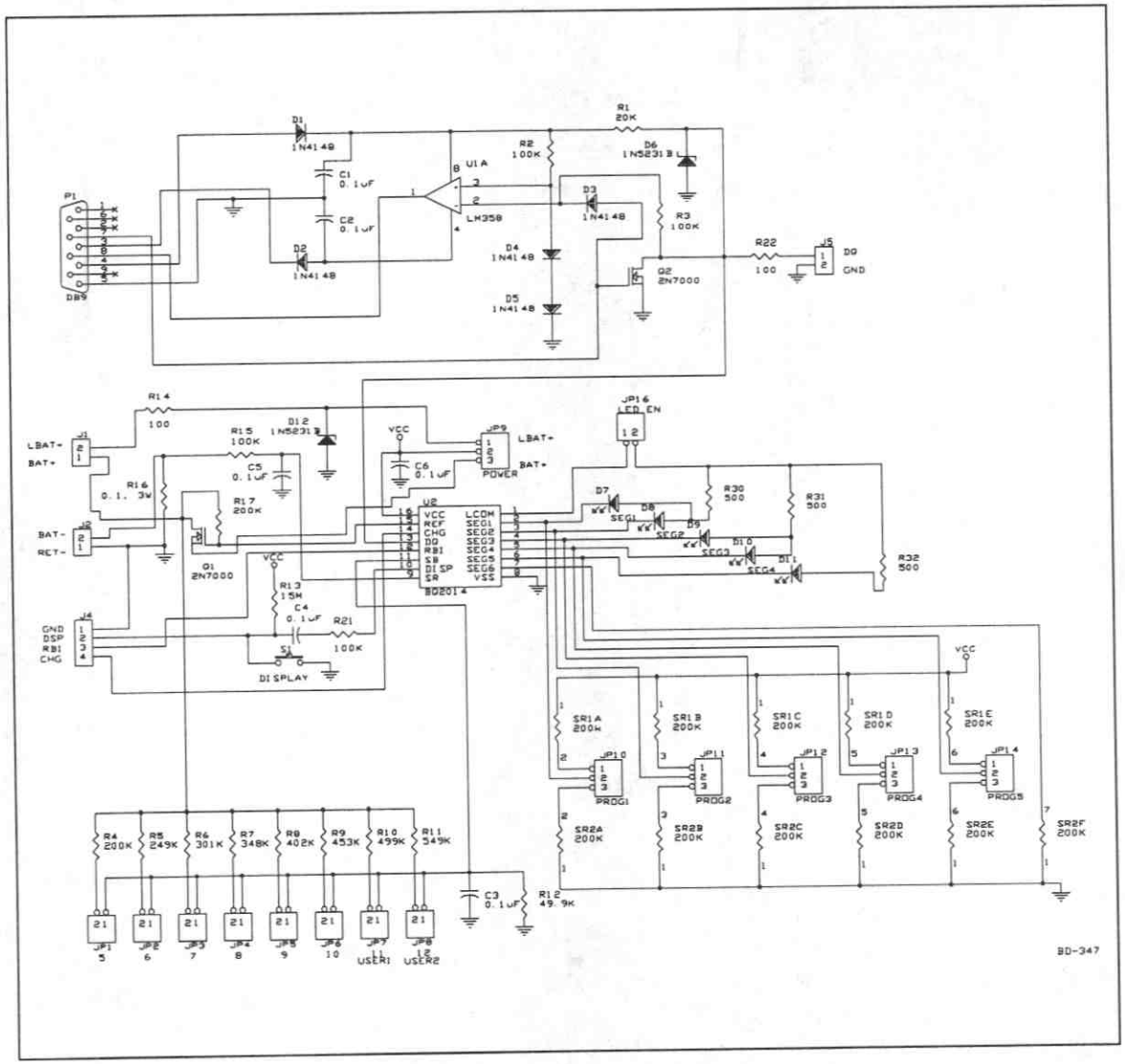
causes the program to write A0 in location 05hex (LMD register).

Appendix B: Troubleshooting

If the EV2014 Main Menu does not appear after starting EV2014, then communication to the bq2014 has not been established. Please check the following:

1. Confirm the proper serial port is being used.
2. Confirm the battery divider is properly set for the number of cells in the battery pack.
3. Confirm JP9 is properly set for either an external supply through LBAT+ (J1) or the microregulator. JP9 closer to Q2 enables the microregulator, while JP9 closer to R13 enables LBAT+. If the battery divider on JP9 is not set properly, the bq2014 will not operate, and the EV2014 UIP or AP14 will not work.
4. Confirm the battery is attached between BAT+ and BAT– (J1 and J2).
5. Push S1. SEG1 LED should be on indicating that the bq2014 is properly powered.
6. If the LED is not on, check the battery voltage on pin 16 of the bq2014 to determine if it is above 3V but below 6.5V.
7. If the LED is on, and the EV2014 Main Menu still does not appear, try using AP14 to establish communication. Appendix A describes AP14.
8. If communication cannot be established using AP14, the problem is either the RS-232 port in the PC or the EV2014 interface section. Please contact Benchmarq if the interface section is not working properly on the EV2014 board.

Appendix C: EV2014 Schematic



Notes

BENCHMARQ

Preliminary **bq2031**

Lead-Acid Fast Charger

Features

- Conforms to battery manufacturers' charge recommendations for cyclic and float charge
- Pulse-width modulation regulator
  - Ideal for high-efficiency switch-mode designs
  - Configurable for linear or gated-current regulation use
- Temperature-compensated voltage reference
- Pin-selectable charge algorithms
  - Two-step constant voltage
  - Dual-level constant current
  - Constant-current pulse
- Pre-charge qualification detects shorted, opened, or damaged cells and conditions battery
- Charging qualified by temperature and voltage limits
- Pin-selectable charge maintenance modes
  - Pulsed current
  - Temperature-compensated float voltage
- Direct LED control outputs display charge status and fault conditions
- Pin-selectable charge termination by maximum threshold voltage, Δ^2V, minimum current, and maximum time

General Description

The bq2031 lead-acid fast-charge IC is designed to optimize charging of lead-acid chemistry batteries. A flexible pulse-width modulation regulator allows the bq2031 to control constant-voltage or constant-current charging. The regulator frequency is set by an external capacitor that offers design flexibility. The switch-mode design keeps power dissipation to a minimum for high-charge-current requirements.

Battery life is extended by temperature-compensated voltage thresholds, which are used during constant-voltage charging to allow continuous float operation over an extended temperature range.

A charge action begins when power is applied or when the battery is replaced. For safety, charging is inhibited until the battery voltage and temperature are within configured limits. If the battery voltage is less than the low-voltage threshold, the bq2031 provides trickle-current conditioning to the battery. The pre-charge conditioning algorithm is based on the SAE J537 charge acceptance test procedure. This prevents high-current bulk charging of possibly damaged or reversed cells.

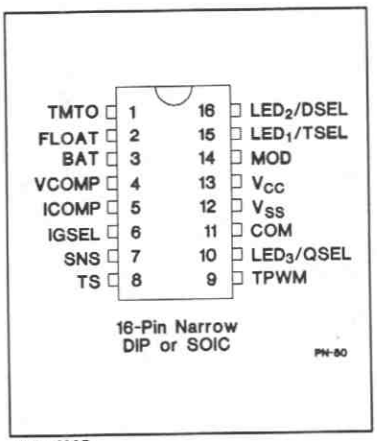
The bq2031 terminates fast charge (bulk charge) based on the battery voltage or charging current conditions.

Bulk charging is terminated by the following:

- Second difference of cell voltage (Δ^2V)
- Minimum cut-off current (MCI)
- Maximum time-out (MTO)
- Maximum threshold voltage (V_{BLK})

After bulk charge, the bq2031 enters a charge maintenance mode (float).

Pin Connections



16-Pin Narrow DIP or SOIC

PN-80

Pin Names

TMTO	Time-out timebase input	LED_3/QSEL	Charge status output 3/ charge regulation select input
FLOAT	State control output		
BAT	Battery voltage input	COM	Common LED output
VCOMP	Voltage loop comp input	V_{SS}	System ground
ICOMP	Current loop comp input	V_{CC}	5.0V±10% power
IGSEL	Current gain select input	MOD	Modulation control output
SNS	Sense resistor input	LED_1/TSEL	Charge status output 1/ Termination select input
TS	Temperature sense input		
TPWM	Regulator timebase input	LED_2/DSEL	Charge status output 2/ Display select input

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Pin Descriptions

TMTO **Time-out timebase input**

This input sets the timebase for maximum charge time. The resistor and capacitor values are determined using the equation on page 6. Figure 2 shows the resistor/capacitor connection.

FLOAT **Float state control output**

This open-drain output uses an external resistor divider network to control the BAT input voltage threshold for the float charge mode. See Figure 1.

BAT **Battery voltage input**

BAT is the battery voltage sense input. This potential is generally developed using a high-impedance resistor divider network connected between the positive and the negative terminals of the battery. See Figure 1 and the equation on page 4.

VCOMP **Voltage loop compensation input**

This input uses an external capacitor for voltage loop stability.

IGSEL **Current gain select input**

This three-state input is used to set I_{MIN}. See Table 4.

ICOMP **Current loop compensation input**

This input uses an external capacitor for current loop stability.

SNS **Charging current sense input**

SNS controls the switching of MOD based on an external sense resistor. See the equation on page 9.

TS **Temperature sense input**

This input is for an external battery temperature monitoring thermistor or probe. The external resistor divider network is set for the lower and upper temperature threshold limits shown in Figure 1.

TPWM **Regulation timebase input**

This input uses an external timing capacitor to set the pulse-width modulation (PWM) frequency. See Figure 2 and the equation on page 9.

COM **Common LED output**

Common output for LED_{1-3}. This output is high impedance during initialization to read program inputs.

QSEL **Charge regulation select input**

This input selects constant- voltage or constant-current regulation mode. See Table 2.

MOD **Current-switching control output**

MOD is a push/pull output that is used to control the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow.

LED_{1-3} **Charger display status 1-3 outputs**

These charger status output drivers are for the direct drive of the LED display. Display modes are shown in Table 3.

DSEL **Display select input**

This three-level input controls the LED_{1-3} charge display modes. See Table 3.

TSEL **Termination select input**

This input controls either constant-current or pulse-current charge modes. See Table 2.

V_{CC} **V_{CC} supply**

5.0V, ± 10% power

V_{SS} **Ground**

Functional Description

Table 1 summarizes the bq2031 operational states. Table 2 describes the bq2031 charge action control pins QSEL and TSEL. The various operational modes of the bq2031 are described in detail in the following sections.

Charge Action Control

The bq2031 initiates a charge when power is applied to V_{CC} or when a battery is replaced. The charge action mode is determined by inputs from the TSEL and QSEL pins. Following charge initiation, the bq2031 checks for acceptable battery temperature (between LTF - low-tem-

Table 1. bq2031 Operational Summary

Charge Action State	Conditions	MOD Output
Battery absent	$V_{CELL} \le V_{INT}$ or $V_{CELL} \ge V_{MCV}$	Low
Charge initiation	V_{CC} applied, $0.8 < V_{CELL} < 0.6 * V_{CC}$.	-
Charge pending	Charge initiation and $V_{TEMP} < V_{HTF}$ or $V_{TEMP} > V_{LTF}$	Low
Pre-charge qualification phase 1	Charge initiation occurred and $V_{TCO} < V_{TEMP} < V_{LTF}$. Voltage regulate V_{CELL} to $V_{FLT} + 0.250V$.	Voltage regulation
Phase 1 fault	$I_{SNS} < I_{COND}$ and charge time > t_{UV1}	-
Phase 1 complete	$I_{SNS} \ge I_{COND}$ and charge time < t_{UV1}	-
Pre-charge qualification phase 2	Phase 1 completed and $V_{HTF} < V_{TEMP} < V_{LTF}$. Current regulate I_{SNS} to I_{COND}.	Current regulation
Phase 2 fault	$V_{CELL} < V_{MIN}$ and charge time > t_{UV2}	-
Phase 2 complete	$V_{CELL} > V_{MIN}$ and charge time > t_{HO1}	-
Two-step voltage regulation mode; QSEL = 0, TSEL = 1, 0		
Fast charge (Bulk charge)	If $V_{CELL} < V_{BLK}$; $I_{SNS} = I_{MAX}$; If $V_{CELL} = V_{BLK}$; $I_{SNS} > I_{MIN}$	Current regulation
Fast charge termination	If $V_{CELL} = V_{BLK}$; $I_{SNS} \le I_{MIN}$ or T_{MTO}	-
Constant voltage maintenance	$V_{CELL} = V_{FLT}$	Voltage regulation
Dual-level constant-current mode; QSEL = 1, TSEL = 0		
Fast charge (Bulk charge)	If $V_{CELL} < V_{BLK}$; Charge-time < T_{MTO}; $\Delta^2V > -8mV$; $I_{SNS} = I_{MAX}$	Current regulation
Fast charge termination	If $V_{CELL} \ge V_{BLK}$; Charge-time < T_{MTO}; $\Delta^2V = -8mV$	-
Constant current maintenance	$I_{SNS} = I_{MIN}$	Current regulation
Pulsed-current mode; QSEL = 1, TSEL = 1		
Fast charge (Bulk charge)	If $V_{CELL} < V_{BLK}$; Charge-time < T_{MTO}, Note (1); $I_{SNS} = I_{MAX}$	Current regulation
Fast charge termination	If $V_{CELL} \ge V_{BLK}$; Charge-time = T_{MTO} (fault)	-
Pulsed current maintenance	If $V_{CELL} \ge V_{FLT}$; Charge suspend; If $V_{CELL} \le V_{FLT}$; Return to bulk charge	MOD = 0

Note:
1. Terminates fast charge and indicates a fault; MOD output = low.
2. $V_{CELL} > V_{MCV}$ indicates fault, MOD output = low.
3. $V_{TEMP} > V_{LTF}$ or $V_{TEMP} < V_{TCO}$ suspends charge action; charge action begins again when $V_{HTF} < V_{TEMP} < V_{LTF}$

Table 2. bq2031 Charge Action Control Summary

Charge Mode	QSEL	TSEL	Fast Charge Termination	Charge Maintenance Action
Two-step/ Constant voltage	Low	High/Low	I_{MIN} or MTO	Voltage regulation at V_{FLT}
Pulsed constant current	High	High	V_{BLK} or MTO[1]	Suspend charge until $V_{CELL} < V_{FLT}$
Dual-level constant current	High	Low	V_{BLK} or Δ^2V or MTO	Current regulation at I_{MIN}

Note: 1. Fault condition

perature fault and HTF - High-temperature fault). The bq2031 then enters a pre-charge qualification phase. After pre-charge qualification, the bq2031 begins fast charge and tests for the following full charge conditions: maximum time out (MTO), $\Delta^2V < -8mV$, minimum current, and maximum threshold voltage. **Note: A temperature fault, $V_{TEMP} > V_{LTF}$ or $V_{TEMP} < V_{TCO}$ (temperature cut-off), will suspend fast charge until the condition is removed.** After fast charge, the bq2031 enters charge maintenance (float) according to the configuration selected by QSEL and TSEL.

Charge Status

Table 3 outlines the various charge states indicated by LED_1, LED_2, and LED_3. In all cases, if the battery voltage at the BAT pin is above the maximum cell voltage (0.6 * V_{CC}), LED_1 and LED_2 outputs are held low, and LED_3 will be high.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are measured for minimum and maximum allowable values. The battery voltage sense input (BAT) for a battery pack should be divided to provide between 0.8V and 0.6 * V_{CC} for proper operation. The resistor-divider ratio is:

$$\frac{R_A}{R_B} = \frac{N * V_{FLT}}{2.2} - 1$$

where N is the number of cells, V_{FLT} is the desired float voltage, R_A is the resistor connected between the positive terminal of the battery and BAT, and R_B is connected to BAT and the battery negative terminal. See Figure 1.

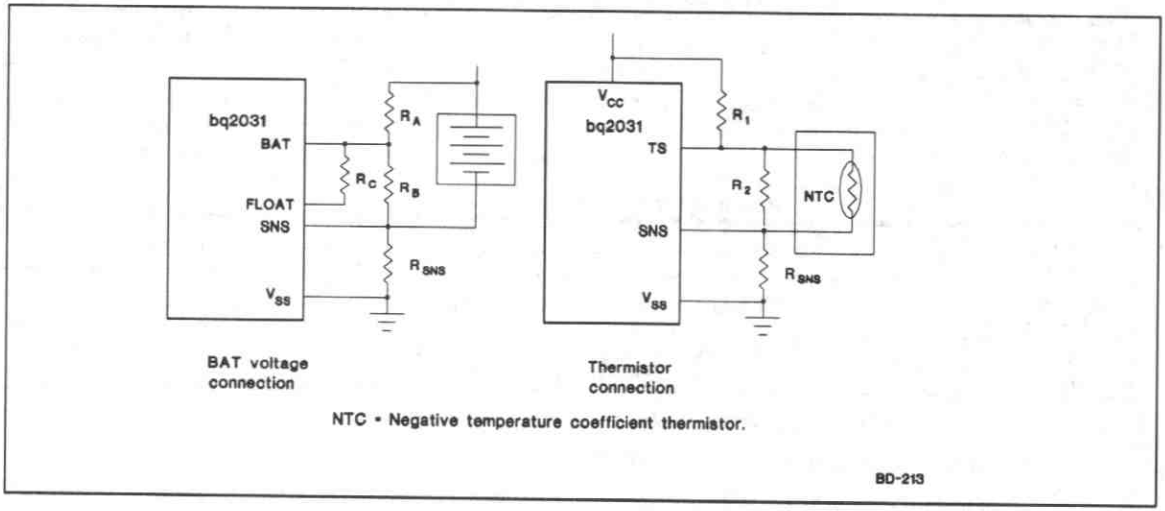


Figure 1. Voltage and Temperature Limit Measurement

V_{BLK} is determined by the following equation:

$$\frac{R_A}{R_B} + \frac{R_A}{R_C} = \frac{N * V_{BLK}}{2.2} - 1$$

where N is the number of cells, V_{BLK} is the desired termination voltage (and constant-voltage regulation point), R_A is the resistor connected between the positive battery terminal and the BAT pin, R_B is the resistor connected between the BAT pin and the negative battery terminal and R_C is the resistor tied between the BAT pin and the float pin. See Figure 1.

Temperature

The bq2031 monitors temperature throughout the charge cycle as a voltage input at the TS pin. Generally, this voltage is developed using an NTC (negative temperature coefficient) thermistor referenced to the SNS pin. The valid voltage range at the TS input for charge initiation is between $0.44 * V_{CC} \le V_{TS} \le 0.6 * V_{CC}$ and is derived using a resistor/thermistor network where R_1 is connected between V_{CC} and the TS pin, R_2 is connected between TS and SNS, and the NTC is connected between TS and SNS. **Note:** The present charge action is suspended if $V_{TEMP} < V_{TCO}$ or $V_{TEMP} > V_{LTF}$, where $V_{TEMP} = V_{TS} - V_{SNS}$. See Figure 1.

The bq2031 recognizes an internal voltage level of $V_{LTF} = 0.6 * V_{CC}$ as the low-temperature fault (LTF) level. If $V_{TEMP} \ge V_{LTF}$, charging is inhibited or suspended until the voltage at TS is once again below V_{LTF}. The bq2031 recognizes an internal voltage level of $V_{HTF} = 0.44 * V_{CC}$ as the high-temperature fault (HTF) level. An internal voltage level of $V_{TCO} = 0.4 * V_{CC}$ is the high temperature cut-off (TCO) limit. If $V_{TEMP} < V_{TCO}$, charging is inhibited or suspended until the voltage at TS is once again above V_{HTF}.

Table 3. bq2031 Display Output Summary

Mode	Charge Action State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	⅛ sec. low, ⅛ sec. high	Low	Low
	Fast charging	High	Low	Low
	Maintenance charging	Low	High	Low
	Charge pending (temperature out of range)	X	X	⅛ sec. low, ⅛ sec. high
	Charging fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	⅛ sec. low, ⅛ sec. high
	Charging fault	X	X	High
DSEL = Float (Mode 3)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	⅛ sec. low, ⅛ sec. high	⅛ sec. low, ⅛ sec. high	Low
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	⅛ sec. low, ⅛ sec. high
	Charging fault	X	X	High

Note: 1 = V_{CC}, 0 = V_{SS}, X = LED state when fault occurred.

Temperature Compensation

The reference used to determine V_{FLT} and V_{BLK} is internally compensated for temperature. The temperature coefficient is –3.9mV/°C, normalized to 25°C. The V_{FLT} and V_{BLK} will vary proportionally by the temperature coefficient as the ambient conditions change.

Battery Removal Detection

Battery removal is sensed by V_{CELL} (V_{BAT} - V_{SNS}) rising above V_{MCV} (0.6 * V_{CC}) or by V_{CELL} falling below V_{INT} (0.8V). An optional external resistor, R_{EXT}, between the battery positive lead and the charging supply pulls V_{CELL} above V_{MCV} to detect battery removal. See Figure 6.

Initiating a Charge Action

A battery charge action is initiated when a battery is inserted or V_{CC} is applied to the bq2031. Battery insertion is recognized when the voltage at the BAT pin falls from above V_{MCV} to below that level, or when the voltage at the BAT pin rises above V_{INT}. When V_{CC} is applied to the bq2031, or when a battery is inserted, a charge action begins after a brief power-on reset period. During this reset period, the states of QSEL, DSEL and TSEL are determined.

Temperature and Voltage Qualification

A fast charge action is qualified by the battery temperature, voltage, and condition. Before fast charge (bulk charge) can begin, the battery temperature must be within preconfigured acceptable limits, and the battery must pass the charge qualification phase.

In the case of a battery that is too warm or too cold, the charge action begins when V_{TEMP} is greater than V_{HTF} and less than V_{LTF}. If the battery temperature is outside the V_{TCO}(0.4 * V_{CC}) or V_{LTF}(0.6 * V_{CC}) limits, the bq2031 enters a charge pending state, and waits until the temperature becomes acceptable.

Once the battery temperature becomes acceptable, the bq2031 tests the battery prior to fast charge. The pre-charge qualification test consists of two phases. During the first phase, the bq2031 applies a constant voltage (V_{FLT} + 0.25V) for a time t_{UV1} (0.02 * t_{MTO}) and measures if the charge current is greater than I_{COND} (maximum charge current divided by 5). If the charge current is greater than I_{COND}, phase 1 is terminated and the bq2031 begins the second phase of the charge acceptance test. If the charge current is not greater than I_{COND} during this time t_{UV1}, then the bq2031 indicates a fault condition and the charge action is terminated.

During the second phase of the pre-charge qualification test, the bq2031 applies a constant current (I_{COND}) for a time t_{UV2} (0.16 * t_{MTO}), and measures if V_{CELL} is greater than V_{MIN} (0.34 * V_{CC}). If V_{CELL} is greater than V_{MIN}, phase 2 is terminated and the bq2031 begins fast charge (bulk). After a brief hold-off time, t_{HO1}, if V_{CELL} is lower than V_{MIN} for greater than time t_{UV2}, the bq2031 indicates a fault condition, and the charge action is terminated.

If V_{TEMP} is above V_{LTF} or V_{TEMP} is below V_{TCO} at any time during a charge cycle, charging is suspended until the battery temperature falls between V_{HTF} and V_{LTF}.

Charge Safety Timer

The bq2031 charge safety timer is set using an external resistor and capacitor as shown in Figure 2.

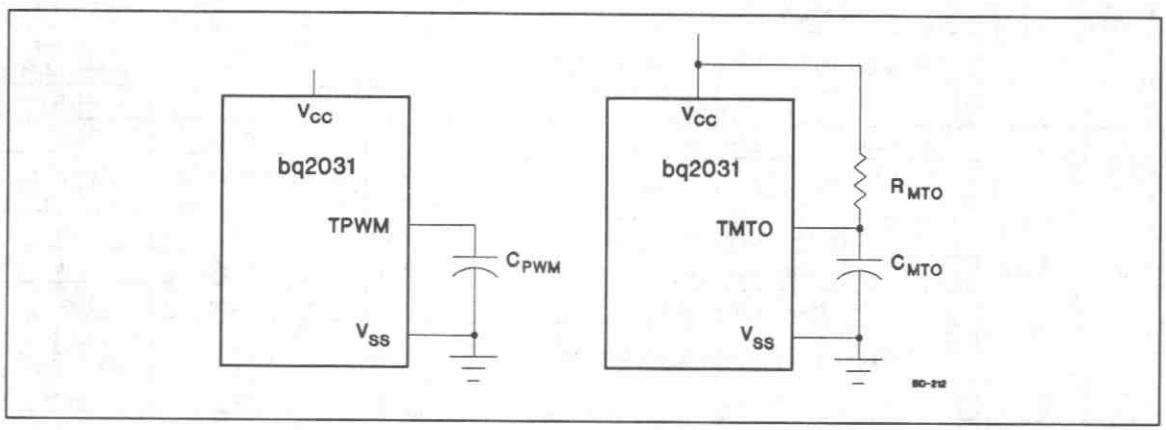


Figure 2. Regulator and Time-out Timebase Circuits

The following equation calculates the charge safety time:

$$t_{MTO}\ (\text{hours}) = [R1\ (K\Omega) * C1(\mu F)] * 0.5$$

where R1 is the resistor value specified in KΩ and C1 is the capacitance specified in µF. A 0.1µf capacitor is typically used for C1.

Fast (Bulk) Charge Termination

Once the battery temperature and voltage prequalifications are met, fast charging (bulk) begins and continues until terminated by one or more of the possible termination conditions:

- Second difference of cell voltage (Δ^2V)
- Minimum cutoff current (MCI)
- Maximum threshold voltage (V_{BLK})
- Maximum time (MTO)

Exceeding the temperature fault limits (V_{LTF}, V_{TCO}) suspends the present charge activity. Charging resumes as soon as the battery temperature becomes acceptable.

Voltage Termination Holdoff

At the start of fast charge, there is a holdoff time during which the Δ^2V and V_{BLK} terminations are disabled. Δ^2V holdoff applies only to the dual-level constant-current modes (QSEL = 1, TSEL = 0). The holdoff time, t_{HO2} is equal to 0.015 * t_{MTO} for fast charging. After t_{HO2}, Δ^2V and V_{BLK} are enabled.

Δ^2V Termination

This mode is enabled if QSEL is high and TSEL is low during initialization, per Table 2. The bq2031 will terminate fast charging (bulk) using a proprietary algorithm which accumulates the decreases in V_{CELL} during charge. The bq2031 makes a Δ^2V termination decision every (0.008 * t_{MTO}) seconds, and terminates when the second difference in cell voltage is less than or equal to –8mV ($\Delta^2V \le -8mV$).

Minimum Cut-off Current (MCI)

This mode is enabled if QSEL is low during initialization per Table 2. The bq2031 will terminate fast charging (bulk) based on the decrease in charge current during constant voltage regulation (V_{BLK}). The minimum current cut-off (MCI) is selectable between $I_{MAX}/10$, $I_{MAX}/20$, and $I_{MAX}/30$ using the IGSEL pin as shown in Table 4. I_{MAX} is the maximum charge current. See the charge current control section on page 9 for configuring the charge current.

Table 4. I_{MIN} Termination Thresholds and Pulse Current Regulation

IGSEL	I_{MIN}
0	$I_{MAX}/10$
1	$I_{MAX}/20$
Z	$I_{MAX}/30$

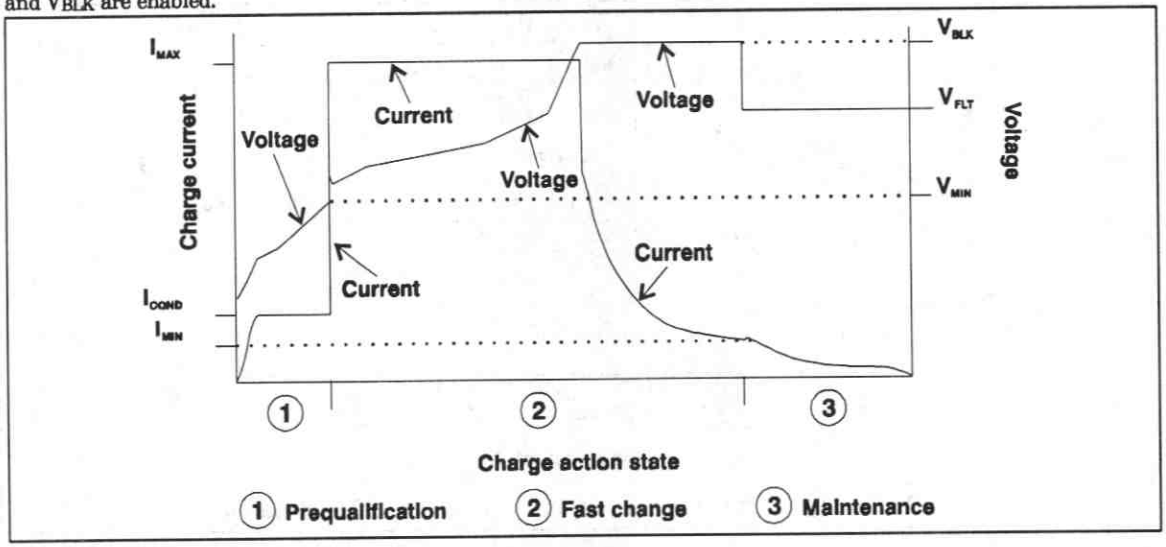


Figure 3. Charging Profile for Constant-Voltage Mode

Maximum Threshold Voltage (V_{BLK})

This mode is enabled when QSEL is high per Table 2. The bq2031 will terminate fast charging (bulk) when V_{CELL} is greater than or equal to V_{BLK}. V_{BLK} is user-selectable per the equations in the section entitled *Battery Voltage and Temperature Measurements* on page 4.

Maximum Time-Out (MTO)

The bq2031 terminates fast charge for exceeding the maximum charge time in all charge modes per Table 2. This timer is reset at the beginning of each state of a charge cycle.

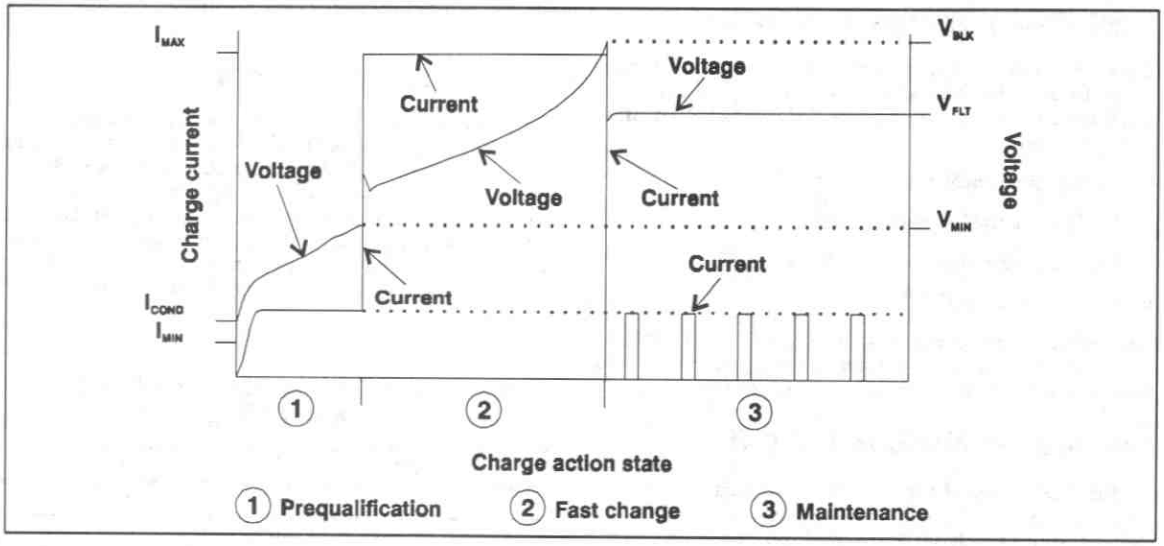


Figure 4. Charging Profile for Constant-Current Mode

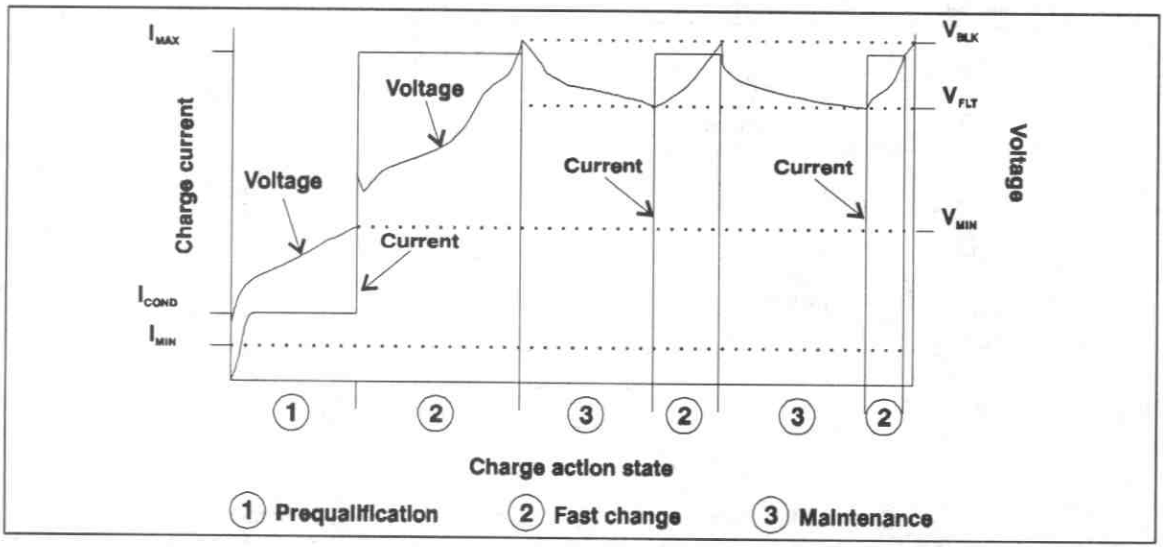


Figure 5. Charging Profile for Constant-Current Pulse Mode

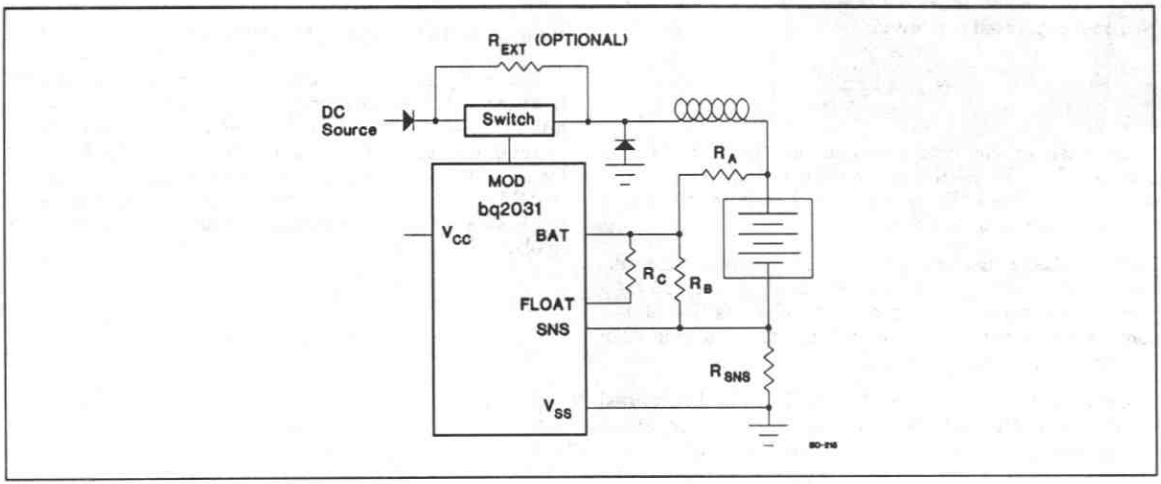


Figure 6. Switch-Mode Buck Regulator Configuration

Charge Maintenance

After fast charge (bulk), the bq2031 enters a charge maintenance state. During charge maintenance, the bq2031 either voltage regulates at V_{FLT}, pulses current at I_{MIN}, or suspends charging until V_{CELL} falls below V_{FLT}. The charge maintenance mode is configured using QSEL and TSEL. See Table 2.

During voltage regulation charge maintenance (QSEL = low), the bq2031 regulates the voltage to maintain V_{FLT}. The bq2031 will continue to test for V_{INT}, V_{MIN}, and V_{MCV} during this mode. **Note:** During voltage regulation, the charge current will not exceed I_{COND}.

During constant-current charge maintenance (QSEL = high, TSEL = low), the bq2031 pulses current at an effective rate of $I_{MAX}/10$, $I_{MAX}/20$, or $I_{MAX}/40$ as programmed by the IGSEL pin. If IGSEL is low, the current is pulsed at I_{COND} for ½ second each second. If IGSEL is high, the current is pulsed for ½ second every 2 seconds. If IGSEL is floating, the current is pulsed for ½ second every 4 seconds. **Note:** During constant-current charge maintenance, the charge voltage will not exceed V_{FLT}. See Table 5.

Figure 5. Constant-Current Charge Maintenance

IGSEL	Pulse Cycle at I_{COND}
0	½ second each second
1	½ second every 2 seconds
Z	½ second every 4 seconds

During current-suspend charge maintenance (QSEL = high, TSEL = high), the charging current is turned off, allowing V_{CELL} to decline to V_{FLT}. When V_{CELL} falls below V_{FLT}, the bq2031 applies a constant current (I_{MAX}) until V_{CELL} reaches V_{BLK}. Once V_{CELL} reaches V_{BLK}, the charge current is again suspended until V_{CELL} falls below V_{FLT}, where the cycle is repeated.

Fault Conditions

The bq2031 uses LED_3 to indicate a variety of fault conditions during the charge cycle. This could be useful in providing battery diagnostics during the charge cycle. A temperature suspend condition is indicated by LED_3 flashing at a ⅛ second rate per Table 3. LED_1 and LED_2 are latched in the state where the temperature suspend condition occurs. If V_{CELL} is above V_{MCV} or below V_{INT}, LED_3 will be high indicating a battery voltage fault. In this case, LED_1 and LED_2 are low.

If a time-out occurs during fast charge prequalification, LED_3 will be high indicating a battery prequalification fault, and LED_1 and LED_2 will indicate charge conditioning state per Table 3. If a timeout occurs during the fast charge phase of pulsed-current charging (QSEL = H, TSEL = H), LED_3 will be high and LED_1 and LED_2 will be latched per Table 3, fast charge section. This indicates a fault condition and terminates fast charging.

Charge Regulation

The bq2031 controls the charge current through the MOD output pin. The bq2031 is designed to support the implementation of a constant-current or constant-voltage regulator, depending on the bq2031 charge configuration. See Figure 6.

Nominal regulated current is:

$$I_{MAX} = \frac{0.275V}{R_{SNS}}$$

When used in this configuration, the charge current is monitored at the SNS input by the voltage drop across the resistor R_{SNS}. R_{SNS} may be chosen to provide a variety of charging currents.

During voltage regulation, the bq2031 monitors the voltage at the BAT pin, and compares it to an internal temperature-compensated reference. The results of the comparison modulates the MOD output pin to maintain the desired voltage at the BAT pin.

The switching frequency of the MOD pin is determined by an externally set time base controlled by a capacitor (C_{PWM}) per the following equation (see Figure 2):

$$F_{PWM(KHz)} = \left(\frac{1}{C_{PWM(\mu F)}} \right) * 10^{-1}$$

The typical value of C_{PWM} is 0.001µF, resulting in a switching frequency of 100KHz.

Frequency Compensation

In order to prevent the voltage or current regulation loop from oscillating, frequency compensation may be required at the VCOMP or ICOMP pins respectively. In general, because of filters in the SNS and BAT feedback loops, a C and/or an RC network is required at the VCOMP and ICOMP pins to add poles and/or zeros to the feedback loop to stabilize regulation. (See the bq2031 application note.)

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec. max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Rating	Unit	Tolerance	Notes
V_{REF}	Internal reference voltage	2.20	V	1%	T_A = 25°C
	Temperature coefficient	-3.9	mV/°C	10%	
V_{LTF}	TS maximum threshold	0.6 • V_{CC}	V	±0.03V	Low temperature fault
V_{HTF}	TS minimum threshold	0.44 • V_{CC}	V	±0.03V	High temperature fault
V_{TCO}	Minimum cutoff voltage	0.4 • V_{CC}	V	±0.03V	Temperature cut-off
V_{MCV}	Maximum cutoff voltage	0.60 * V_{CC}	V	±0.03V	
V_{MIN}	Under-voltage threshold at BAT	0.34 * V_{CC}	V	±0.03V	
V_{INT}	Charge initiation threshold	0.8	V	±0.03V	
V_{SNS}	Current sense at SNS	0.27	V	10%	V_{MAX}
		0.05	V	10%	V_{MIN}

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
I_{CC}	Supply current	-	2	4	mA	Outputs unloaded
I_{IZ}	DSEL tri-state open detection	-2	-	2	µA	Note 2
	IGSEL tri-state open detection	-2		2	µA	
V_{IH}	Logic input high	V_{CC}-1.0	-	-	V	QSEL,TSEL
		V_{CC}-0.3	-	-	V	DSEL, IGSEL
V_{IL}	Logic input low	-	-	V_{SS}+1.0	V	QSEL,TSEL
		-	-	V_{SS}+0.3	V	DSEL, IGSEL
V_{OH}	LED_1, LED_2 ,LED_3, output high	V_{CC}-0.8	-	-	V	$I_{OH} \leq 10mA$
	MOD output high	V_{CC}-0.8	-	-	V	$I_{OH} \leq 5mA$
V_{OL}	LED_1, LED_2 ,LED_3, output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 10mA$
	MOD output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 5mA$
	FLOAT output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 5mA$, Note 3
	COM output low	-	-	V_{SS}+0.5	V	$I_{OL} \leq 30mA$
I_{OH}	LED_1, LED_2 ,LED_3, source	-10	-	-	mA	V_{OH} =V_{CC}-0.5V
	MOD source	-5.0	-	-	mA	V_{OH} =V_{CC}-0.5V
I_{OL}	LED_1, LED_2 ,LED_3, sink	10	-	-	mA	V_{OL} = V_{SS}+0.5V
	MOD sink	5	-	-	mA	V_{OL} = V_{SS}+0.8V
	FLOAT sink	5	-	-	mA	V_{OL} = V_{SS}+0.8V, Note 3
	COM sink	30	-	-	mA	V_{OL} = V_{SS}+0.5V
I_{IL}	DSEL logic input low source	-	-	+30	µA	V = V_{SS} to V_{SS}+ 0.3V, Note 2
	IGSEL login input low source	-	-	+70	µA	V = V_{SS} to V_{SS}+ 0.3V
I_{IH}	DSEL logic input high source	-30	-	-	µA	V = V_{CC} - 0.3V toV_{CC}
	IGSEL logic input high source	-70	-	-	µA	V = V_{CC} - 0.3V toV_{CC}
I_L	Input leakage	-	-	±1	µA	QSEL, TSEL, Note 2

Notes: 1. All voltages relative to V_{SS}.

2. Conditions during initialization after V_{CC} applied.

3. SNS = 0V

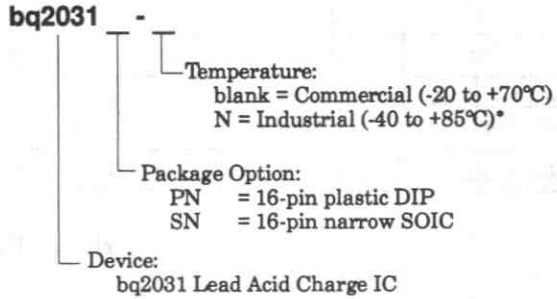
Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{BATZ}	Battery input impedance	50	-	-	MΩ	
R_{SNSZ}	SNS input impedance	50	-	-	MΩ	
R_{TSZ}	TS input impedance	50	-	-	MΩ	
R_{PROG1}	Soft-programmed pull-up or pull-down resistor value (for programming)	-	-	10	KΩ	DSEL, TSEL, and QSEL
R_{PROG2}	Pull-up or pull-down resistor value	-	-	3	KΩ	IGSEL
R_{MTO}	Charge timer resistor	20	-	480	KΩ	C_{MTO} = 0.1µF, Maximum recommended value

Timing (TA = TOPR; VCC = 5V ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{MTO}	Charge timer time-out range	1	-	24	hours	See Figure 1
t_{UV1}	Conditioning time-out current sense period	-	$0.02t_{MTO}$	-	-	
t_{UV2}	Conditioning time-out voltage sense period	-	$0.16t_{MTO}$	-	-	
t_{DV}	$-\Delta^2V$ termination sample time period	-	$0.008t_{MTO}$	-	-	
$t_{HOLDOFF1}$	Conditioning state 2 holdoff time period	-	$0.002t_{MTO}$	-	-	
$t_{HOLDOFF2}$	Bulk-charge hold-off time period	-	$0.015t_{MTO}$	-	-	
F_{PWM}	Regulator timebase frequency range	-	100		KHz	See Figure 1, Equation 2
	External C_{PWM} range	-	0.001	-	µF	

Ordering Information



* Contact factory for availability.

Gas Gauge IC With SMBus Interface

Features

- Provides conservative and repeatable measurement of available charge in NiCd, NiMH, and Lithium Ion rechargeable batteries
- Designed for battery pack integration
  - 120µA typical standby current
  - Small size enables implementations in as little as 1/2 square inch of PCB
- Supports Rev. 0.95 System Management Bus interface and Smart Battery Data specifications
- Measurements compensated for current and temperature
- Contains self-discharge compensation using internal temperature sensor
- Internal time base eliminates external resonator or crystal
- 16-pin narrow DIP or SOIC

General Description

The bq2040 Gas Gauge IC With SMBus Interface is intended for battery-pack or in-system installation to maintain an accurate record of a battery's available charge. The bq2040 directly supports NiCd, NiMH, and Lithium Ion battery chemistries. Other battery chemistries will be supported with future variations of the device.

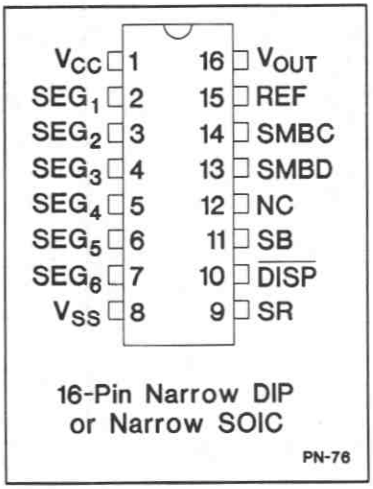
The bq2040 supports the System Management Bus (SMBus) protocol and the Smart Battery Data (SBData) specifications. Battery voltage, temperature, state-of-charge, capacity, charge-cycle count, etc. are available over the SMBus serial link. Battery-charge state can be directly indicated using a five- or six-segment LED display to graphically depict battery full-to-empty in 20% increments.

The bq2040 estimates battery self-discharge based on an internal timer and temperature sensor. The bq2040 applies compensations for battery temperature and rate of charge or discharge to the charge, discharge, and self-discharge calculations, providing available charge information across a wide range of operating conditions. The bq2040 automatically recalibrates, or "learns" battery capacity in the full course of a discharge cycle from full to empty.

The bq2040 may operate directly from 3 or 4 nickel chemistry cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} for other battery cell configurations.

An external E^2PROM is used to program initial values into the bq2040. Values such as design capacity, chemistry, and serial number, can be customized for individual battery pack configurations.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-76

Pin Names

V_{OUT}	Supply output	SB	Battery sense input
SEG_1	LED segment 1	$\overline{DISP}$	Display control input
SEG_2	LED segment 2	SR	Sense resistor input
SEG_3	LED segment 3	SMBC	Serial communication clock
SEG_4	LED segment 4	SMBD	Serial communication data input/output
SEG_5	LED segment 5		
SEG_6	LED segment 6	V_{CC}	3.0-6.5V
REF	Voltage reference output	V_{SS}	System ground

Pin Descriptions

SEG_1–SEG_6 **LED display segment outputs**

Each output may activate an external LED to sink the current sourced from V_{CC}.

SMBC **System management bus clock**

This open-drain bi-directional pin is used to clock the data transfer to and from the bq2040.

SMBD **System management bus data**

This open-drain bi-directional pin is used to transfer address and data to and from the bq2040.

SCL **Serial clock (shared with SEG_1)**

This output is used to clock the data transfer between the bq2040 and the external configuration memory.

SDA **Serial data and address (shared with SEG_2)**

This bi-directional pin is used to transfer address and data to and from the bq2040 and the external configuration memory.

NC **No connect**

V_{OUT} **Supply output**

This output supplies power to the external E^2PROM configuration memory, if present. Do not connect this pin if you are not using the external memory.

SR **Sense resistor input**

The voltage drop (V_{SR}) across pins SR and V_{SS} is monitored and integrated over time to interpret charge and discharge activity. The SR input is connected to the sense resistor and the negative terminal of the battery. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2040 is $V_{SR} + V_{OS}$ (see Table 3 on page 8).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ floating allows the LED display to be active during charge or during discharge if the rate is greater than a user-programmable threshold. $\overline{DISP}$ low activates the display.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2040 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2040 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2040 using the LED capacity display, the serial port, and an optional external E^2PROM for battery pack programming information. The bq2040 can be configured for battery chemistry, manufacturer name and serial number, display mode, self-discharge compensation, and various other battery-specific information. Table 1 outlines the externally programmable functions available in the bq2040.

An internal temperature sensor eliminates the need for an external thermistor—reducing cost and components. An internal, temperature-compensated time-base eliminates the need for an external oscillator, further reducing cost and components. The entire circuit in Figure 1 could occupy less than ¾ square inch of board space.

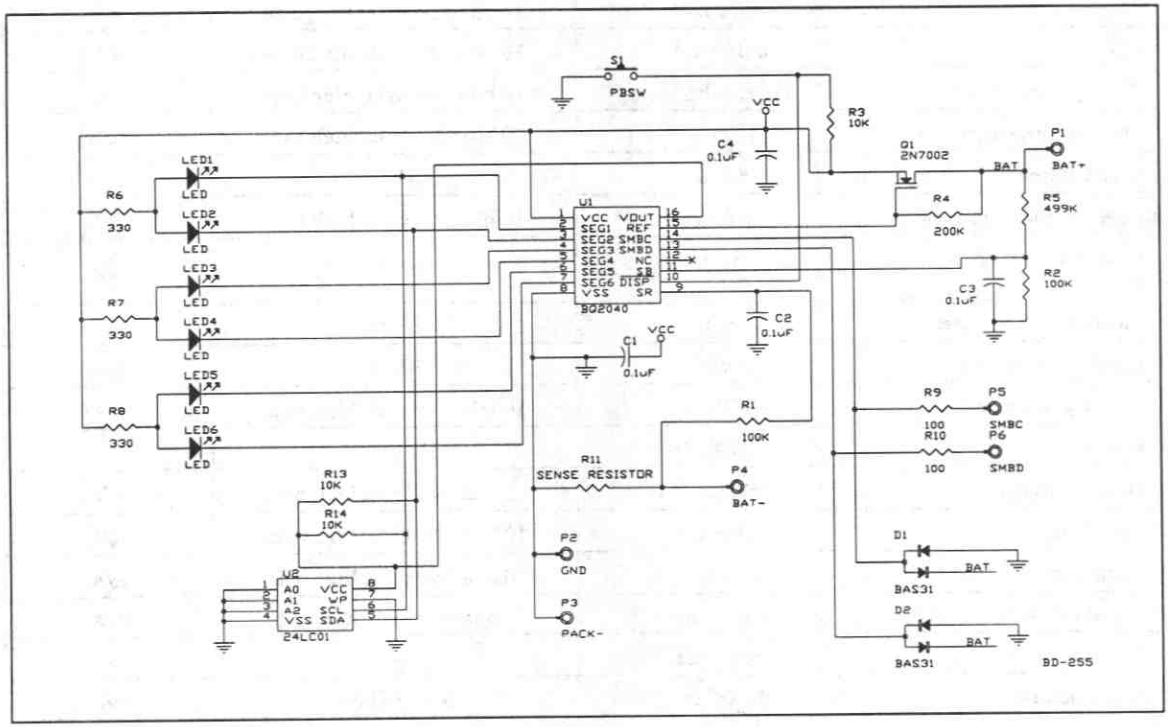


Figure 1. Battery Pack Application Diagram—LED Display

Table 1. Configuration Memory Programming Values

Parameter Name	Address	Length	Units
Design capacity	0x00/0x01	16 bits: low byte, high byte	mAh
Initial battery voltage	0x02/0x03	8 bits	N/A
Fast charging current	0x04/0x05	16 bits: low byte, high byte	mA
Charging voltage	0x06/0x07	16 bits: low byte, high byte	mV
Remain capacity alarm	0x08/0x09	16 bits: low byte, high byte	N/A
FLAGS1	0x0a	8 bits	N/A
FLAGS2	0x0b	8 bits	N/A
Current measurement gain	0x0c/0x0d	16 bits: low byte, high byte	N/A
EDV_1	0x0e/0x0f	16 bits: low byte, high byte	mV
EDV_F	0x10/0x11	16 bits: low byte, high byte	mV
Temperature offset	0x12/0x13	16 bits: low byte, high byte	°K
Self-discharge rate	0x14	16 bits: low byte, high byte	N/A
Digital filter	0x15	8 bits	N/A
Current integration gain	0x16/0x17	16 bits: low byte, high byte	N/A
Discharge display threshold	0x18	8 bits	N/A
Battery voltage offset	0x19	8 bits	mV
Battery voltage gain	0x1a	8 bits	N/A
Slow charging current	0x1b/0x1c	16 bits: low byte, high byte	mA
Reserved	0x1d/0x31	-	-
Design voltage	0x32/0x33	16 bits: low byte, high byte	mV
Specification info	0x34/0x35	16 bits: low byte, high byte	N/A
Manufacturer date	0x36/0x37	16 bits: low byte, high byte	N/A
Serial number	0x38/0x39	16 bits: low byte, high byte	N/A
Reserved	0x3a/0x3f	-	-
Manufacturer name	0x40/0x4f	8 + 120 bits	N/A
Device name	0x50/0x5f	8 + 120 bits	N/A
Chemistry	0x60/0x6f	8 + 120 bits	N/A
Manufacturer data	0x70/0x7f	8 +120 bits	N/A

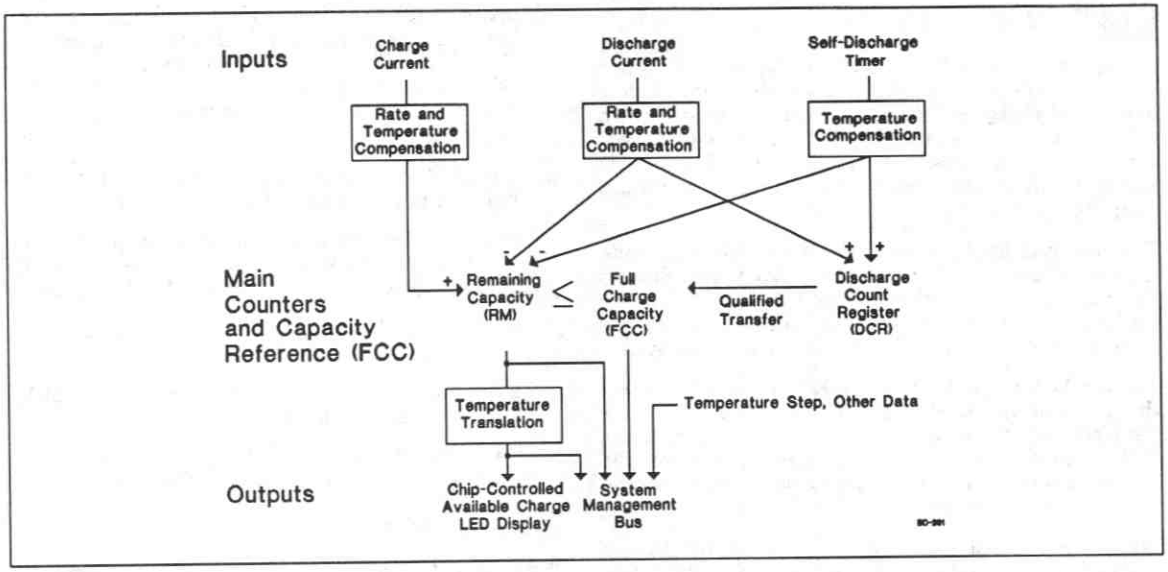


Figure 2. Operational Overview

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2040 monitors the battery potential through the SB pin. The voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{R_5}{R_2} = \frac{MBV}{2.25} - 1$$

where MBV is the maximum battery voltage, R_5 is connected to the positive battery terminal, and R_2 is connected to the negative battery terminal. R_5/R_2 should be rounded to the next highest integer. The battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV) and for alarm warning conditions. EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging. The battery voltage gain is programmed via E^{2}PROM.

Two EDV thresholds for the bq2040 are externally programmable.

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

EDV monitoring may be disabled under certain conditions. If the discharge current is greater than 3A, EDV monitoring is disabled and resumes after the current falls below 1.5A.

Reset

The bq2040 is reset when first connected to the battery pack; the bq2040 can also be reset with a command over the serial port.

Temperature

The bq2040 monitors temperature using an internal sensor. The temperature is used to adapt charge/discharge and self-discharge compensations. Temperature may also be accessed over the serial port.

Layout Considerations

The bq2040 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C1, C3, and C4) should be placed as close as possible to the SB and V_{CC} pins, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor (C2) should be placed as close as possible to the SR pin.
- The sense resistor (R_{11}) should be as close as possible to the bq2040.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2040. The bq2040 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature-compensated and charge is rate-compensated. Self-discharge is only temperature compensated.

The main counter, Remaining Capacity (RM), represents the available battery capacity at any given time. Battery charging increments the RM register, while battery discharging and self-discharge decrement the RM register and increment the DCR (Discharge Count Register).

The Discharge-Count Register (DCR) is used to update the Full-Charge Capacity (FCC) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2040 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Design Capacity (DC). Until FCC is updated, RM counts up to, but not beyond, this threshold during subsequent charges.

1. **Full-Charge Capacity or learned-battery capacity:**

   FCC is the last measured discharge capacity of the battery. On initialization (application of V_{CC}), FCC = DC. During subsequent discharges, the FCC is updated with the latest measured capacity in the Discharge Count Register (DCR), representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the FCC register. The FCC also serves as the 100% reference threshold used by the relative display mode.

2. **Design Capacity (DC):**

   The DC is the user specified battery capacity and is programmed by using an external E^2PROM or by writing data over the serial port if the E^2PROM is not present. The DC also provides the 100% reference for the absolute display mode.

3. **Remaining Capacity (RM):**

   RM counts up during charge to a maximum value of FCC and down during discharge and self-discharge to 0. RM is reset to 0 on initialization and when EDV1 = 1. To prevent overstatement of charge during periods of overcharge, RM stops incrementing when RM = FCC.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of RM and can continue increasing after RM has decremented to 0. Prior to RM = 0 (empty battery), both discharge and self-discharge increment the DCR. After RM = 0, only discharge increments the DCR. The DCR resets to 0 when RM = FCC. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new FCC value on the first charge after a valid discharge to V_{EDV1} if:

   - No valid charge initiations (charges greater than 10mAh, where $V_{SRO} > V_{SRQ}$) occurred during the period between RM = FCC and EDV1 detected.
   - The self-discharge count is not more than 256mAh.
   - The temperature is ≥ 273°K when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for FCC update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2040 increments RM at a rate proportional to V_{SRO} and, if enabled, activates an LED display. Charge actions increment the RM after compensation for charge rate and temperature.

The bq2040 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 10 mAh. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the RM register to decrement and the DCR to increment. Exceeding the user-programmable discharge display threshold, stored in external E^2PROM, activates the display, if enabled. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The bq2040 continuously decrements RM and increments DCR for self-discharge based on time and temperature. The self-discharge rate is dependent on the battery chemistry. The bq2040 self-discharge estimation rate is externally programmed in E^2PROM and can be programmed from 0 to 25% per day at 20°C. This rate doubles every 10°C from 0°C to 70°C.

Count Compensations

The bq2040 determines fast charge when the charge rate exceeds the programmed fast charge rate. Charge activity is compensated for temperature and rate before updating the RM and/or DCR. Discharge rate is compensated for temperature before updating the RM register. Self-discharge estimation is compensated for temperature before updating RM or DCR.

Charge Compensation

Charge efficiency is compensated for rate, temperature, and battery chemistry. For Li-ion chemistry cells, the charge efficiency is unity for all cases. However, the charge efficiency for nickel chemistry cells is adjusted using the following equation:

$$Q_{EFF} = Q_{EB} + 0.125 * \frac{AverageCurrent()}{FullCapacity()}$$

where $Q_{EB} = 0.80$ if $T < 30°C$

$Q_{EB} = 0.75$ if $30°C \le T < 40°C$

$Q_{EB} = 0.60$ if $T \ge 40°C$

and AverageCurrent() $\le$ FullCapacity()

$Q_{EFF} = Q_{EB} + 0.125$ if AverageCurrent() > FullCapacity()

Digital Magnitude Filter

The bq2040 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. Table 2 shows typical digital filter settings. The proper digital filter setting can be calculated using the following equation.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 * V_{SRD}$$

Table 2. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The FCC is susceptible to error on initialization or if no updates occur. On initialization, the FCC value includes the error between the design capacity and the actual capacity. This error is present until a valid discharge occurs and FCC is updated (see the DCR description on page 6). The other cause of FCC error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

Remaining Capacity Compensation

The bq2040 adjusts the RM as a function of temperature. This adjustment accounts for the reduced capacity of the battery at colder temperatures. The following equation is used to adjust RM:

If $T \ge 5°C$

RemainingCapacity () = NominalAvailableCapacity()

If $T < 5°C$

RC() = NAC() (1 + TCC * (T - 5°C))

where T = temperature °C

TCC = 0.016 for Li-Ion cells

TCC = 0.0004 for Ni chemistry cells

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the RM register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Display

The bq2040 can directly display capacity information using low-power LEDs. The bq2040 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the FCC. Each LED segment represents 20% of the FCC. The sixth segment, SEG_6, is not used.

In absolute mode, each segment represents a fixed amount of charge, based on the initial design capacity. In absolute mode, each segment represents 20% of the design capacity, with SEG_6 representing "overfull" (charge above the design capacity). As the battery wears out over time, it is possible for the FCC to be below the initial design capacity. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The displayed capacity is compensated for the present battery temperature. The displayed capacity will vary as temperature varies, indicating the available charge at the present conditions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-6} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2040 recognizes a valid charge or if the discharge rate exceeds the programmed fast discharge display threshold. When pulled low, the segment outputs become active immediately for a period of approximately 4 seconds.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2, 4, and 6. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} ($EDV_1 = 1$), indicating a low-battery condition. V_{SB} below V_{EDVF} ($EDV_F = 1$) disables the display output.

Microregulator

The bq2040 can operate directly from 3 or 4 nickel chemistry cells. To facilitate the power supply requirements of the bq2040, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2040 can be inexpensively built using the FET and an external resistor; see Figure 1.

Communicating With the bq2040

The bq2040 includes a simple two-pin (SMBC and SMBD) serial data interface. A host processor uses the interface to access various bq2040 registers. This allows battery characteristics to be easily monitored, by adding two contacts to the battery pack. The open-drain SMBD and SMBC pins on the bq2040 are pulled up by the host system, or may be connected to V_{SS}, if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends the smart battery address and an eight-bit command byte to the bq2040. The command directs the bq2040 to either store the next data received to a register specified by the command byte or output the data specified by the command byte.

bq2040 Data Protocols

The SMBus Host, acting in the role of an SMBus master, uses the read word and write word protocols to communicate integer data with the bq2040. The read block protocol is used to access block data, such as ManufacturerName(). When the bq2040 needs to inform the SMBus Host about an alarm condition or to inform the Smart Battery Charger about its desired charging voltage or current, the bq2040, acting as an SMBus master, uses the write word protocol to communicate with the SMBus Host or Smart Battery Charger acting as an SMBus slave.

Table 3. bq2040 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP} = V_{CC}$.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

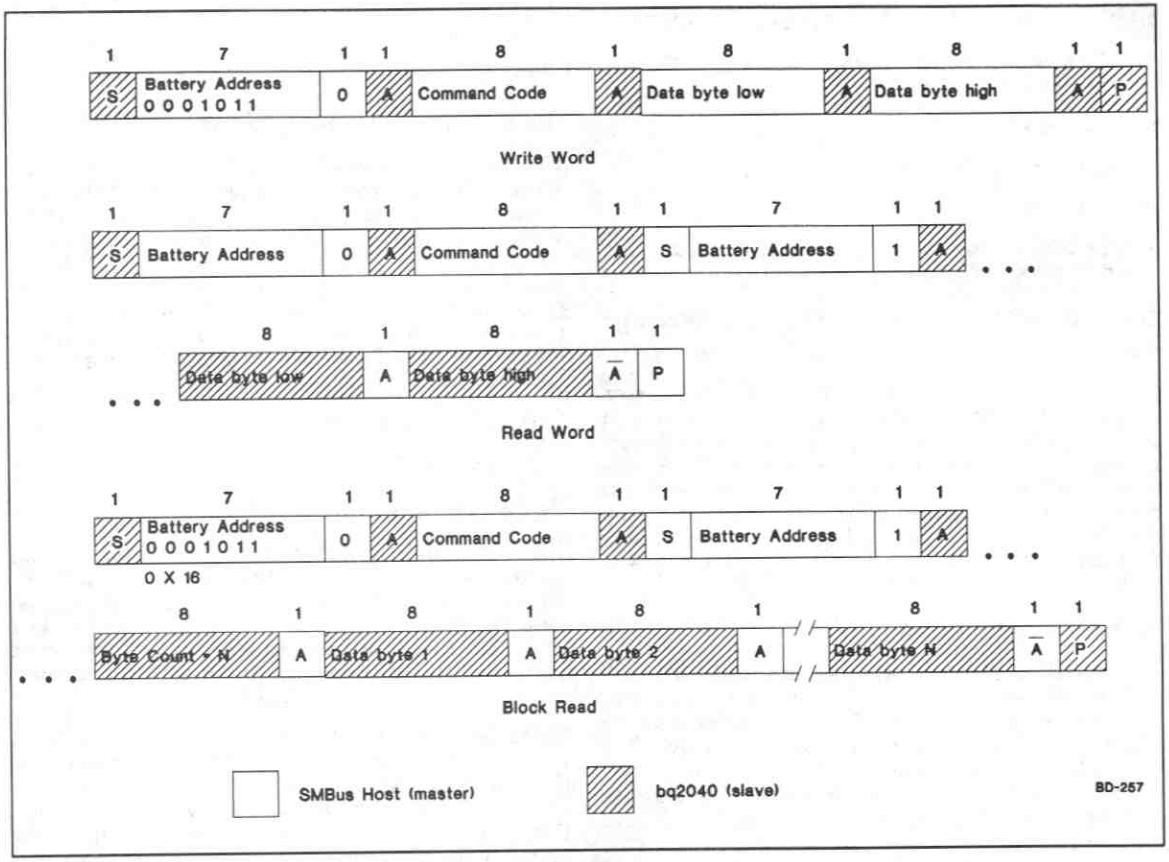


Figure 3. SMBus Host Protocols

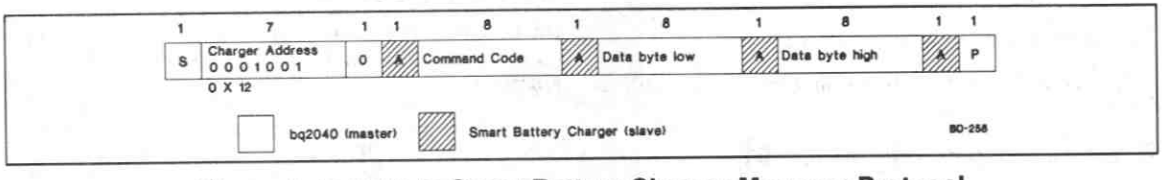


Figure 4. bq2040-to-Smart Battery Charger Message Protocol

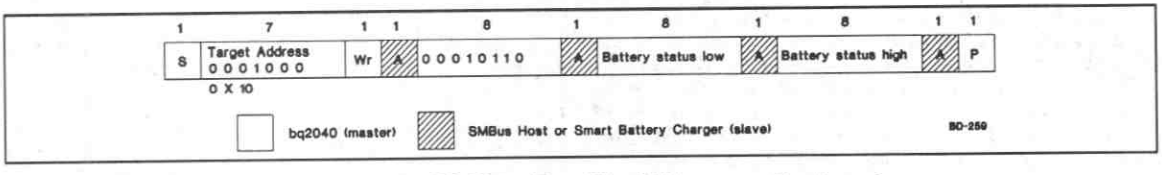


Figure 5. bq2040-to-Bus Host Message Protocol

SMBus Host-to-bq2040 Message Protocol

The SMBus Host communicates with the bq2040 using one of three protocols:

- Read word
- Write word
- Read block

The particular protocol used is a function of the command. The protocols used are shown in Figure 3.

bq2040-to-Smart Battery Charger Message Protocol

The bq2040, acting as an optional SMBus master, sometimes tries to alter the charging characteristics. It also may send critical messages to the Smart Battery Charger, behaving as an SMBus slave using the SMBus write word protocol. Communication begins with the Smart Battery Charger's address, followed by a command code and a two-byte value. The Smart Battery Charger adjusts its output to correspond with the request. See Figure 4.

bq2040 Critical Message Protocol

The bq2040 to SMBus Host message is sent using the SMBus write word protocol. Communication begins with the SMBus Host's address, followed by the bq2040's address, which also replaces the command code. The SMBus Host or Smart Battery Charger can now determine that the bq2040 was the originator of the message and that the following 16 bits are its status. See Figure 5.

SMBus Host-to-Smart Battery Messages (see Table 7)

ManufacturerAccess() (0x00)

This read or write word is optional and its meaning is implementation specific.

RemainingCapacityAlarm() (0x01)

This read or write word sets or gets the LowCapacity threshold value. Whenever the RemainingCapacity() falls below the RemainingCapacity alarm value, the Smart Battery sends AlarmWarning() messages to the SMBus Host with the REMAINING_CAPACITY_ALARM bit set. A value of 0 disables this alarm. The value is set to 10% of the design capacity at time of manufacture. The value will remain unchanged until altered by the RemainingCapacityAlarm() function.

Units: mAh

Range: 0 to 65,535 mAh

RemainingTimeAlarm() (0x02)

This read/write word sets or gets the RemainingTime alarm value. Whenever the AverageTimeTo Empty() falls below the RemainingTime value, the Smart Battery sends AlarmWarning() messages to the SMBus Host with the REMAINING_TIME_ALARM bit set. A RemainingTime value of 0 disables this alarm. The RemainingTime alarm is set to 10 minutes at the time of manufacture. The RemainingTime alarm value may be changed until altered by the RemainingTimeAlarm() function.

Units: Minutes

Range: 0 to 65,535 minutes

BatteryMode() (0x03)

This read/write word selects the various battery operational modes. The bq2040 supports the battery's capacity information specified in mAh. This function also determines whether the ChargingCurrent() and ChargingVoltage() values are broadcast to the Smart Battery Charger when the Smart Battery requires charging (CHARGER_MODE bit).

CHARGER_MODE bit enables or disables the Smart Battery's transmission of ChargingCurrent() and ChargingVoltage() messages to the Smart Battery Charger. When set, the Smart Battery will *not* transmit ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger. When cleared, the Smart Battery will transmit the ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger when charging is desired.

CAPACITY_MODE bit indicates that capacity information will be reported in mAh and current is in mA units.

Field	Bits Used	Format	Allowable Values
Reserved	0–13		
CHARGER_MODE	14	bit flag	0-Enable broadcast to charger 1-Disable broadcast to charger
CAPACITY_MODE	15	bit flag	0-Report in mA or mAh

AtRate() (0x04)

This read/write word is the first half of a two-function set used to set the AtRate value used in calculations made by the AtRateTimeToFull(), and AtRateTimeTo Empty().

- When the AtRate value is positive, the AtRateTimeTo-Full() function returns the predicted time to full-charge at the AtRate value of charge.
- When the AtRate value is negative, the AtRateTimeTo Empty() function returns the predicted operating time at the AtRate value of discharge.

Units: mA

Range: -32,768 mA to 32,767 mA

Note: The AtRate value is set to zero at time of manufacture (default).

AtRateTimeToFull() (0x05)

This read-only word returns the predicted remaining time to fully charge the battery at the AtRate value (mA).

Units: minutes

Range: 0 to 65,534 min

Granularity: 2 min or better

Invalid Data Indication: 65,535 indicates the battery is not being charged

AtRateTimeToEmpty() (0x06)

This read-only word returns the predicted remaining operating time if the battery is discharged at the AtRate value.

Units: minutes

Range: 0 to 65,534 min

Granularity: 2 min or better

Invalid Data Indication: 65,535 indicates the battery is not being discharged

AtRateOK() (0x07)

This read-only word returns a Boolean value that indicates whether or not the EDV_1 flag has been set.

Boolean: Indicates if the battery can supply additional energy

Units: Boolean

Range: TRUE ≠ 0 ,FALSE= 0

Temperature() (0x08)

This read-only word returns the cell-pack's internal temperature (°K).

Output: unsigned int—cell temperature in tenths of degrees Kelvin increments

Units: 0.1°K

Range: 0 to +500.0°K

Granularity: 0.5°K or better

Accuracy: ±3°K

Voltage() (0x09)

This read-only word returns the cell-pack voltage (mV).

Output: unsigned int—battery terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

Granularity: 0.2% of design voltage

Accuracy: ±0.2% of design voltage

Current() (0x0a)

This read-only word returns the current through the battery's terminals (mA).

Output: signed int—charge/discharge rate in mA —positive for charge, negative for discharge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for discharge

Granularity: 0.2% of the DesignCapacity() or better

Accuracy: ±0.2% of the Design Capacity

AverageCurrent() (0x0b)

This read-only word returns a rolling average of the current through the battery's terminals. The AverageCurrent() function returns meaningful values after the battery's first minute of operation.

Output: signed int—charge/discharge rate in mA — positive for charge, negative for discharge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for discharge

Granularity: 0.2% of the DesignCapacity() or better

Accuracy: ±0.2% of the Design Capacity

MaxError() (0x0c)

This read-only word returns the expected margin of error (%).

Output: unsigned int—percent uncertainty

Units: %

Range: 0 to 100%

Granularity: 1% or better

RelativeStateOfCharge() (0x0d)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity() (%).

Output: unsigned int—percent of remaining capacity

Units: %

Range: 0 to 100%

Granularity: 1% or better

AbsoluteStateOfCharge() (0x0e)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of DesignCapacity() (%). Note that AbsoluteStateOfCharge can return values greater than 100%.

Output: unsigned int—percent of remaining capacity

Units: %

Range: 0 to 65,535 %

Granularity: 1% or better

Accuracy: ±MaxError()

RemainingCapacity() (0x0f)

This read-only word returns the predicted remaining battery capacity. The RemainingCapacity() value is expressed in mAh at the nominal discharge rate.

Output: unsigned int—estimated remaining capacity in mAh

Units: mAh

Range: 0 to 65,535 mAh

Granularity: 0.2% of DesignCapacity() or better

FullChargeCapacity() (0x10)

This read-only word returns the predicted pack capacity when it is fully charged. The FullChargeCapacity() value is expressed in mAh at a C/5 discharge rate.

Output: unsigned int—estimated full charge capacity in mAh or 10mWh

Units: mAh

Range: 0 to 65,535 mAh

Granularity: 0.2% of design capacity or better

RunTimeToEmpty() (0x11)

This read-only word returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty() value is calculated based on Current().

Output: unsigned int—minutes of operation left

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is being charged

AverageTimeToEmpty() (0x12)

This read-only word returns the predicted remaining battery life at the present average discharge rate (minutes). The AverageTimeToEmpty is calculated based on AverageCurrent().

Output: unsigned int—minutes of operation left

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is being charged

AverageTimeToFull() (0x13)

This read-only word returns the predicted time until the Smart Battery reaches full charge at the present average charge rate (minutes).

Output: unsigned int—remaining time in minutes

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is not being charged

BatteryStatus() (0x16)

This read-only word returns The Smart Battery's status word (flags). Some of the BatteryStatus() flags (REMAINING_CAPACITY_ALARM and REMAINING_TIME_ALARM) are calculated based on current. See Table 4. for definitions.

unsigned int: Status Register with alarm conditions bit mapped as follows:

Alarm Bits	
0x8000	OVER_CHARGED_ALARM
0x4000	TERMINATE_CHARGE_ALARM
0x2000	DTEMP_ALARM
0x1000	OVER_TEMP_ALARM
0x0800	TERMINATE_DISCHARGE_ALARM
0x0400	reserved
0x0200	REMAINING_CAPACITY_ALARM
0x0100	REMAINING_TIME_ALARM
Status Bits	
0x0080	INITIALIZED
0x0040	DISCHARGING
0x0020	FULLY_CHARGED
0x0010	FULLY_DISCHARGED
Error Code	
0x0000–0x000f	reserved for error codes

CycleCount() (0x17)

This read-only word returns the number of charge/discharge cycles the battery has experienced. A charge/discharge cycle starts from a base value equivalent to the battery's state-of-charge, upon completion of a charge cycle. The bq2040 increments the cycle counter during the current charge cycle, if the battery has been discharged to below 85% of the state-of-charge at the end of the last charge cycle. A discharge > 0.5% prevents false reporting of small charge/discharge cycles.

Output: unsigned int—count of charge/discharge cycles the battery has experienced

Units: cycles

Range: 0 to 65,535 cycles; 65,535 indicates battery has experienced 65,535 or more cycles

Granularity: 1 cycle

DesignCapacity() (0x18)

This read-only word returns the theoretical capacity of a new pack. The DesignCapacity() value is expressed in mAh at the nominal discharge rate.

Output: unsigned int—battery capacity in mAh

Units: mAh

Range: 0 to 65,535 mAh

DesignVoltage() (0x19)

This read-only word returns the theoretical voltage of a new pack (mV).

Output: unsigned int—the battery's normal terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

SpecificationInfo() (0x1a)

This read-only word returns the version number of the SmartBattery specification the battery pack supports, as well as voltage and current scaling information in packed integer. The SpecificationInfo is packed as follows: (major version number • 0x10 + minor version number) + (voltage scaling + current scaling • 0x10) • 0x100.

Field	Bits Used	Format	Allowable Value
Revision	0–3	4-bit binary value	0–15
Version	4–7	4-bit binary value	0–15
VScale	8–11	4-bit binary value	0–3 (multiples voltage by 10 ^ VScale)
IPScale	12–15	4-bit binary value	0–3 (multiples current/power by 10 ^ IPScale)

ManufactureDate() (0x1b)

This read-only word returns the date the cell was manufactured in a packed integer word. The date is packed as follows: (year - 1980), month, day.

Field	Bits Used	Format	Allowable Value
Day	0–4	5-bit binary value	1–31 (corresponds to date)
Month	5–8	4-bit binary value	1–12 (corresponds to month number)
Year	9–15	7-bit binary value	0 • 127 (corresponds to year biased by 1980)

SerialNumber() (0x1c)

This read-only word returns a serial number. This number, when combined with the ManufacturerName(), the DeviceName(), and the ManufactureDate(), uniquely identifies the battery (unsigned int).

Output: unsigned int

ManufacturerName() (0x20)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The character string contains the battery manufacturer's name. For example, "BattCorp" identifies the Smart Battery manufacturer as BattCorp.

Output: string—character string

DeviceName() (0x21)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's name. For example, a DeviceName() of "MBC301" indicates that the battery is a model BC301.

Output: string—character string

DeviceChemistry() (0x22)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's chemistry. For example, if the DeviceChemistry() function returns "NiMH," the battery pack contains nickel metal hydride cells.

Output: string—character string

ManufacturerData() (0x23)

This read-only string allows access to an up to 15-byte manufacturer data string.

Output: block data—data whose meaning is assigned by the Smart Battery's manufacturer

bq2040 or SMB Host-to-Smart Battery Charger Messages(See Table 6)

Whenever the BatteryMode() CHARGER_MODE bit is set to zero (default) and the bq2040 detects the presence of a Smart Battery Charger (level 2 charger—refer to the Smart Battery Charger Specification), the bq2040 sends the ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger. The bq2040 continues broadcasting these values at whatever interval it deems appropriate to maintain correct charging. For example, the bq2040 detects the presence of a Smart Battery Charger by recognizing a charge current. See BatteryMode().

ChargingCurrent() (0x14)

The bq2040 sends the desired charging rate to the Smart Battery Charger (mA).

Output: unsigned int—maximum charger output current in mA

Units: mA

Range: 0 to 65,534 mA

Granularity: 0.2% of the design capacity or better

Accuracy: -± 0.2% of the design capacity

Invalid data indication: 65,535 indicates the Smart Battery Charger should operate as a voltage source outside its maximum regulated current range

ChargingVoltage() (0x15)

The bq2040 sends the desired voltage to the Smart Battery Charger (mV).

Output: unsigned int—charger output current in mV

Units: mV

Range: 0 to 65,534 mV

Granularity: 0.2% of the design voltage or better

Accuracy: -± 0.2% of the design voltage

Invalid data indication: 65,535 indicates the Smart Battery Charger should operate as a current source outside its maximum regulated voltage range

bq2040 Critical Messages

Whenever the bq2040 detects a critical condition, it becomes a bus master and sends AlarmWarning() messages to both the Smart Battery Charger, if enabled, and the SMBus Host, as appropriate, notifying them of the critical condition(s). The message sent by the AlarmWarning() function is similar to the message returned by the BatteryStatus() function. The bq2040 continues broadcasting the AlarmWarning() messages at 10-second intervals until the critical condition(s) has been corrected.

AlarmWarning() (0x16)

The bq2040, acting as a bus master device to the SMBus Host and/or the Smart Battery Charger, sends this message to notify them that one or more alarm conditions exist. Alarm indications are encoded as bit fields in the Battery's status, which is then sent to the SMBus Host and/or Smart Battery Charger by this function. The AlarmWarning() is repeated at 10-second intervals until the condition(s) causing the alarm has been corrected.

Output: unsigned int—Status Register with alarm conditions bit mapped as follows:

Alarm Bits	
0x8000	OVER_CHARGED_ALARM
0x4000	TERMINATE_CHARGE_ALARM
0x2000	DTEMP_ALARM
0x1000	OVER_TEMP_ALARM
0x0800	TERMINATE_DISCHARGE_ALARM
0x0400	reserved
0x0200	REMAINING_CAPACITY_ALARM
0x0100	REMAINING_TIME_ALARM
Status Bits	
0x0080	INITIALIZED
0x0040	DISCHARGING
0x0020	FULLY_CHARGED
0x0010	FULLY_DISCHARGED
Error Code	
0x0000–0x000f	All bits set high prior to AlarmWarning() transmission

Note: Alarm bits 0x0200 and 0x0100 cause the AlarmWarning() to be sent only to the SMBus Host. All other alarm bits cause the AlarmWarning() to be sent to both the SMBus Host and the Smart Battery Charger, if CHARGER_MODE = 0.

Status Bits and Error Codes

Status bits are listed in Table 4 and error codes are listed in Table 5.

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Table 4. Status Bits

Alarm Bits		
Bit Name	**Set When:**	**Reset When:**
OVER_CHARGED_ALARM	bq2040 detects that it is being charged beyond an end-of-charge indication	bq2040 detects that it is no longer being overcharged
TERMINATE_CHARGE_ALARM **Note:** Failure to correct the problem may result in permanent damage to the battery.	bq2040 detects that one or more of its charging parameters are out of range (for example, its voltage or current is too high)	Parameter falls back into the allowable range
DTEMP_ALARM	bq2040 detects that the rate of its internal thermal rise ($\Delta T/\Delta t$) is greater than 1.25°C/min	Rate of thermal rise falls back into the acceptable range (T < 50°C)
OVER_TEMP_ALARM	bq2040 detects that its internal temperature is greater than 60°C	Internal temperature falls back into the acceptable range
TERMINATE_DISCHARGE_ALARM	bq2040 determines that it has supplied all the charge that it can without being damaged (that is, continued use will result in permanent capacity loss to the battery)	Battery reaches a state of charge sufficient for it to once again safely supply power
REMAINING_CAPACITY_ALARM	bq2040 detects that the RemainingCapacity() is less than that set by the RemainingCapacity() function	Either the value set by the RemainingCapacityAlarm() function is lower than the Remaining Capacity() or the RemainingCapacity() is increased by charging
REMAINING_TIME_ALARM	bq2040 detects that the estimated remaining time at the present discharge rate is less than that set by the RemainingTimeAlarm() function	Either the value set by the RemainingTimeAlarm() function is lower than the AverageTimeToEmpty() or the AverageTimeToEmpty() is increased by charging
Status Bits		
Bit Name	**Set When:**	**Reset When:**
INITIALIZED	bq2040 is set when the bq2040 has reached a full or empty state	Battery detects that power-on or user-initiated reset has occurred
DISCHARGING	bq2040 determines that it is not being charged	Battery detects that it is being charged
FULLY_CHARGED	bq2040 determines that it has reached a charge termination point	Battery may be charged again
FULLY_DISCHARGED	bq2040 determines that it has supplied all the charge that it can without being damaged (that is, continued use will result in permanent capacity loss to the battery)	RelativeStateOfCharge() is greater than or equal to 20%

Table 5. Error Codes

Error	Code	Access	Description
OK	0x0000	read/write	bq2040 processed the function code without detecting any errors
Busy	0x0001	read/write	bq2040 is unable to process the function code at this time
NotReady	0x0002	read/write	bq2040 can not read or write the data at this time—try again later
UnsupportedCommand	0x0003	read/write	bq2040 does not support the requested function code
AccessDenied	0x0004	write	bq2040 detected an attempt to write to a read-only function code
Overflow/Underflow	0x0005	read/write	bq2040 detected a data overflow or underflow
BadSize	0x0006	write	bq2040 detected an attempt to write to a function code with an incorrect size data block
UnknownError	0x0007	read/write	bq2040 detected an unidentifiable error

Table 6. bq2040 Master Functions

Function	Code	Access	Data
ChargingCurrent (to Smart Battery Charger)	0x14	write	mA
ChargingVoltage (to Smart Battery Charger)	0x15	write	mV
AlarmWarning (to SMBus Host)	0x16	write	word
AlarmWarning (to Smart Battery Charger)	0x16	write	word

Table 7. Smart Battery Slave Functions

Function	Code	Access	Units	Defaults
ManufacturerAccess	0x00	read/write	word	
RemainingCapacityAlarm	0x01	read/write	mAh	0.1* DC
RemainingTimeAlarm	0x02	read/write	minutes	000Ah
BatteryMode	0x03	read/write	bit flags	0000h
AtRate	0x04	read/write	mA	0000h
AtRateTimeToFull	0x05	read	minutes	FFFFh
AtRateTimeToEmpty	0x06	read	minutes	FFFFh
AtRateOK	0x07	read	Boolean	0000h
Temperature	0x08	read	0.1°K	-
Voltage	0x09	read	mV	-
Current	0x0a	read	mA	0000h
AverageCurrent	0x0b	read	mA	0000h
MaxError	0x0c	read	percent	2%
RelativeStateOfCharge	0x0d	read	percent	0000h
AbsoluteStateOfCharge	0x0e	read	percent	0000h
RemainingCapacity	0x0f	read	mAh	0000h
FullChargeCapacity	0x10	read	mAh	E^2
RunTimeToEmpty	0x11	read	minutes	-
AverageTimeToEmpty	0x12	read	minutes	-
AverageTimeToFull	0x13	read	minutes	-
ChargingCurrent	0x14	read	mA	E^2
ChargingVoltage	0x15	read	mV	E^2
BatteryStatus	0x16	read	bit flags	0050h
CycleCount	0x17	read	count	0000h
DesignCapacity	0x18	read	mAh	E^2
DesignVoltage	0x19	read	mV	E^2
SpecificationInfo	0x1a	read	unsigned int	E^2
ManufactureDate	0x1b	read	unsigned int	E^2
SerialNumber	0x1c	read	number	E^2
Reserved	0x1d - 0x1f	-	-	-
ManufacturerName	0x20	read	string	E^2
DeviceName	0x21	read	string	E^2
DeviceChemistry	0x22	read	string	E^2
ManufacturerData	0x23	read	string	E^2

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2040 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (T_A = T_{OPR}; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
E_{VSB}	Battery voltage error relative to SB	-30mV	-	30mV	V	See note

Note: The accuracy of the voltage measurement may be improved by adjusting the battery voltage offset, stored in external E^2PROM. For proper operation, V_{CC} should be 1.5V greater than V_{SB}.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 6.5V
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LVOUT}	V_{OUT} output leakage	-0.2	-	0.2	µA	E^2PROM off
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	1.4	-	5.5	V	SCL, SDA, SMBC, SMBD
V_{IL}	Logic input low	-0.5	-	0.6V	V	SCL, SDA, SMBC, SMBD
V_{OL}	Data, clock output low	-	-	0.4	V	I_{OL}=350µA, SDA, SMBD
I_{OL}	Sink current	100	-	350	µA	V_{OL}≤0.4V, SDA, SMBD
V_{OLSL}	SEGx output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG1–SEG6
V_{OLSH}	SEGx output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG1–SEG6
V_{OHVL}	V_{OUT} output, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{VOUT} = -5.25mA
V_{OHVH}	V_{OUT} output, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{VOUT} = -33.0mA
I_{VOUT}	V_{OUT} source current	-33	-	-	mA	At V_{OHVH} = V_{CC} - 0.6V
I_{OLS}	SEGx sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V

Note: All voltages relative to V_{SS}.

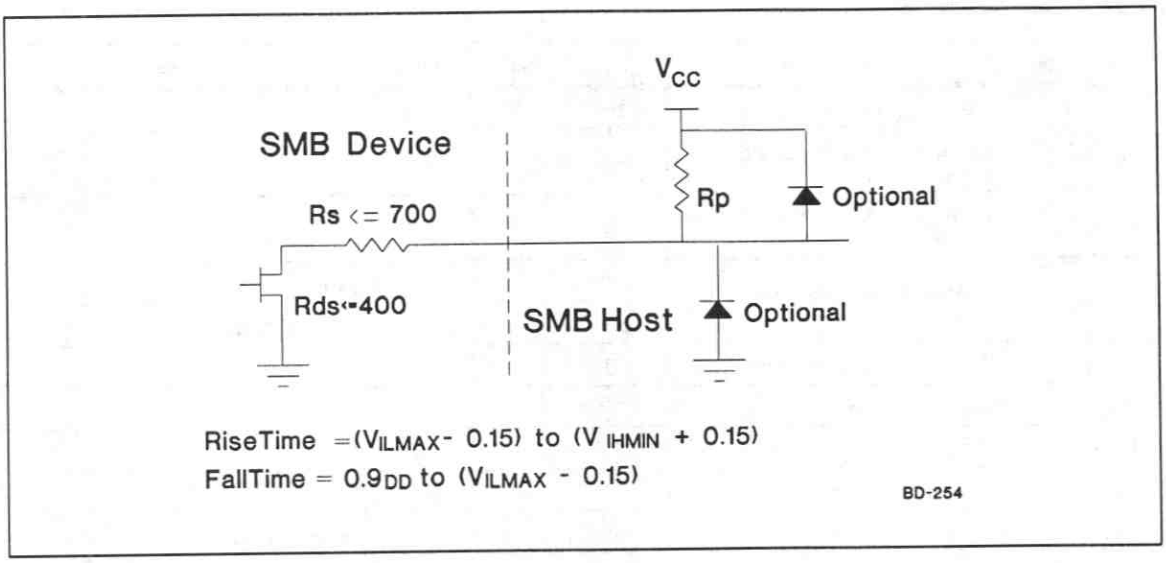


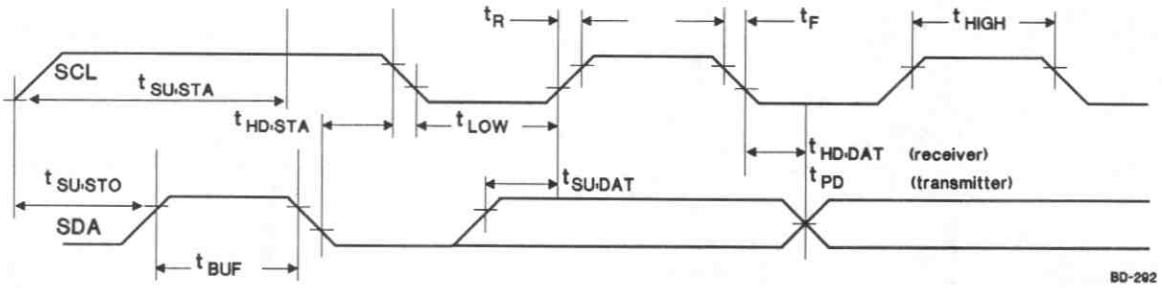
Figure 6. AC Test Conditions

AC Specifications

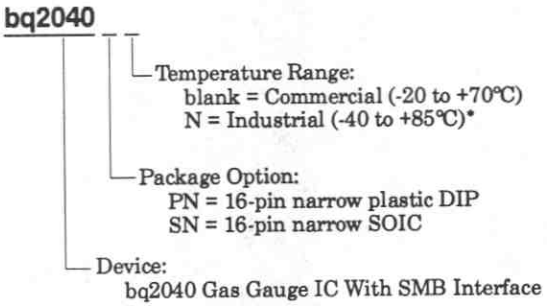
Symbol	Parameter	Min	Max	Units	Notes
F_{SMB}	SMBus operating frequency	10	100	KHz	
T_{BUF}	Bus free time between stop and start condition	4.7		µs	
$T_{HD:STA}$	Hold time after (repeated) start condition	4.0		µs	
$T_{SU:STA}$	Repeated start condition setup time	250		ns	SMBD
		4.7		µs	External Memory
$T_{SU:STO}$	Stop condition setup time	4.0		µs	
$T_{HD:DAT}$	Data hold time	0		ns	
$T_{SU:DAT}$	Data setup time	250		ns	
T_{HOG}	Message buffering time		20	ms	
T_{PD}	Data output delay time	300	3500	ns	External memory only. See Note.
T_{LOW}	Clock low period	4.7		µs	
T_{HIGH}	Clock high period	4.0		µs	
T_F	Clock/Data fall time		300	ns	
T_R	Clock/data rise time		1000	ns	

Note: The external memory must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Bus Timing Data



Ordering Information



* Contact factory for availability.

Notes

BENCHMARQ

bq2050

Lithium Ion Power Gauge™ IC

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Features

- Conservative and repeatable measurement of available capacity in Lithium Ion rechargeable batteries
- Designed for battery pack integration
  - 120µA typical operating current
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- 16-pin narrow DIP or SOIC

General Description

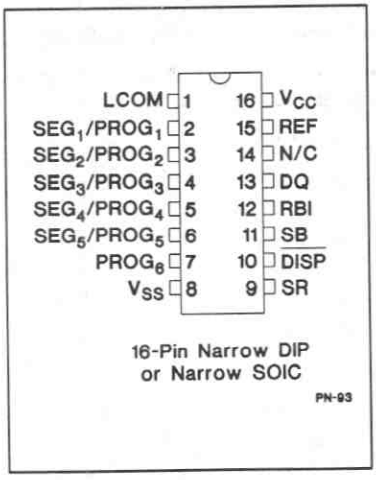
The bq2050 Lithium Ion Power Gauge™ IC is intended for battery-pack or in-system installation to maintain an accurate record of the battery's available capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

Nominal available capacity may be directly indicated using a five- or six-segment LED display. These segments are used to graphically ndicate available capacity. The bq2050 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2050 outputs battery information in response to external commands over the serial link.

The bq2050 may operate directly from one cell (V_{BAT} > 3V). With the REF output and an external transistor, a simple, inexpensive regulator can be built for systems with more than one series cell.

Internal registers include available capacity, temperature, scaled available energy, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2050 power gauge data registers.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

PN-93

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ program 1 input	N/C	No connect
$SEG_2/PROG_2$	LED segment 2/ program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ program 3 input	RBI	Register backup input
$SEG_4/PROG_4$	LED segment 4/ program 4 input	SB	Battery sense input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	DISP	Display control input
$PROG_6$	Program 6 input	SR	Sense resistor input
		Vcc	3.0–6.5V
		Vss	System ground

Pin Descriptions

LCOM — **LED common output**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 — **LED display segment outputs (dual function with $PROG_1$–$PROG_6$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ — **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ — **Power gauge rate selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ — **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the self-discharge and battery compensation factors as shown in Table 1.

$PROG_6$ — **Capacity initialization selection**

This three-level pin defines the battery state of charge at reset as shown in Table 1.

N/C — **No connect**

SR — **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor Rs is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied between the negative terminal of the battery and the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2050 is $V_{SR} + V_{OS}$.

$\overline{DISP}$ — **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during charge. $\overline{DISP}$ low activates the display. See Table 1.

SB — **Secondary battery input**

This input monitors the battery cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

RBI — **Register backup input**

This pin is used to provide backup potential to the bq2050 registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

DQ — **Serial I/O pin**

This is an open-drain bidirectional pin.

REF — **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} — **Supply voltage input**

V_{SS} — **Ground**

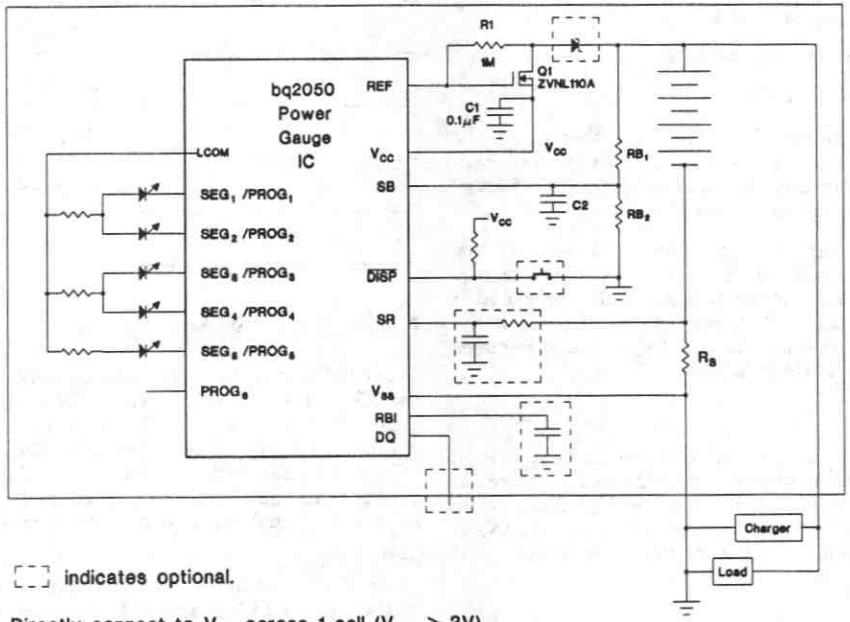
Functional Description

General Operation

The bq2050 determines battery capacity by monitoring the amount of current input to or removed from a rechargeable battery. The bq2050 measures discharge and charge currents, measures battery voltage, estimates self-discharge, monitors the battery for low battery voltage thresholds, and compensates for temperature and charge/discharge rates. The current measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The estimate of scaled available energy is made using the remaining average battery voltage during the discharge cycle and the remaining nominal available charge. The scaled available energy measurement is corrected for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2050 using the LED display capability as a charge-state indicator. The bq2050 is configured to display capacity in relative display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. A push-button display feature is available for momentarily enabling the LED display.

The bq2050 monitors the charge and discharge currents as a voltage across a sense resistor (see Rs in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



[ ] indicates optional.

Directly connect to V_{CC} across 1 cell (V_{BAT} > 3V).

Otherwise, R1, C1, and Q1 are needed for regulation of > 1 cell.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required, application-specific.

A series Zener may be used to limit discharge current at low voltages in designs using 3 or more cells.

BD-316

Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2050 monitors the battery potential through the SB pin. The voltage is determined through a resistor-divider network per the following equation:

$$\frac{RB1}{RB2} = 2N - 1$$

where N is the number of cells, RB1 is connected to the positive battery terminal, and RB2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2050 are programmable with the default values fixed at:

EDV1 (early warning) = 1.52V

EDVF (empty) = 1.47V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. The V_{SB} value is also available over the serial port.

During discharge and charge, the bq2050 monitors V_{SR} for various thresholds used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if the discharge rate is greater than 2C (typical) and resumes ½ second after the rate falls below 2C.

RBI Input

The RBI input pin is intended to be used with a storage capacitor or external supply to provide backup potential to the internal bq2050 registers when V_{CC} drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V. A diode is recommended to isolate the external supply, if necessary.

Reset

The bq2050 can be reset by issuing a command over the serial port as described on page 14.

Temperature

The bq2050 internally determines the temperature in 10°C steps centered from approximately -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown in the following table:

TMP (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2050 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C1 and C2) should be placed as close as possible to the V_{CC} and SB pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (R_S) should be as close as possible to the bq2050.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2050. The bq2050 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2050 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

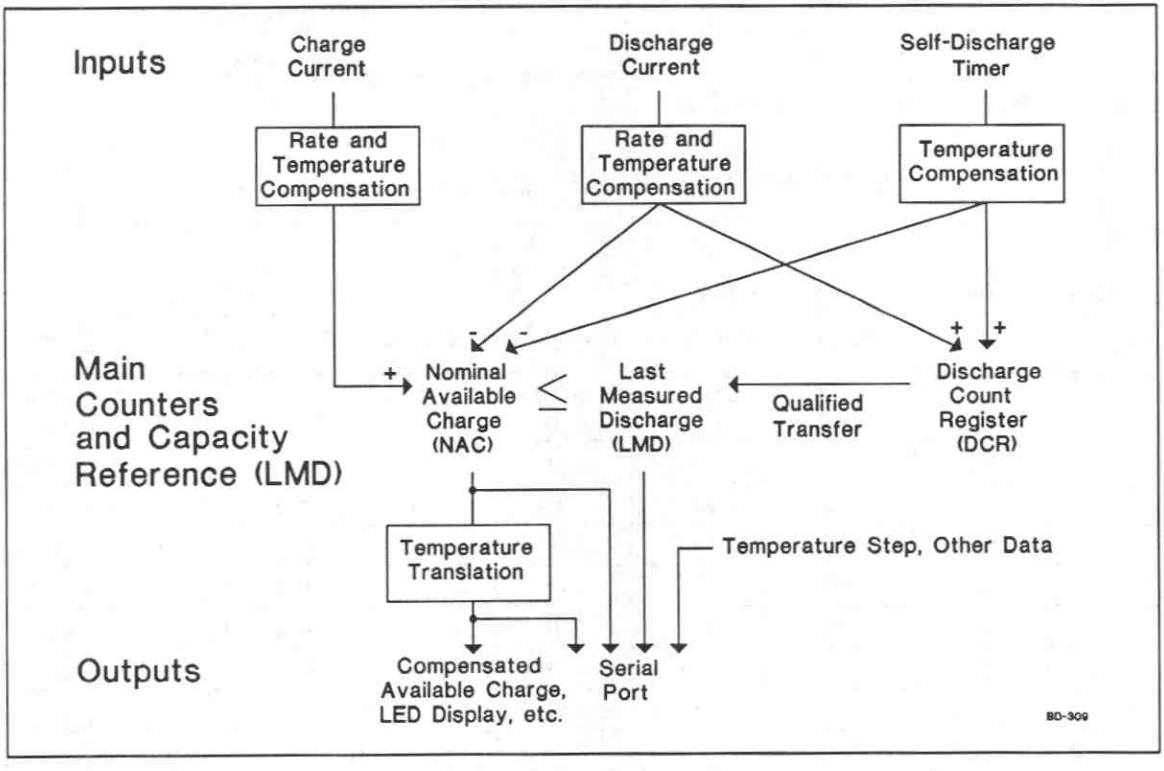


Figure 2. Operational Overview

2. Programmed Full Count (PFC) or initial battery capacity:

The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2050 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) • sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference until the bq2050 "learns" a new capacity reference.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.05Ω
Number of cells = 2
Capacity = 1000mAh, Li-Ion battery, coke-anode
Current range = 50mA to 1A
Relative display mode
Serial port only
Self-discharge = $NAC/_{512}$ per day @ 25°C
Voltage drop over sense resistor = 2.5mV to 50mV
Nominal discharge voltage = 3.6V

Table 1. bq2050 Programming

Pin Connection	$PROG_5$ Compensation/ Self-Discharge	$PROG_6$ NAC on Reset	$\overline{DISP}$ Display State
H	Table 4/Disabled	PFC	LEDs disabled
Z	Table 4/ $NAC/_{512}$	0	LEDs on when charging
L	Table 3/ $NAC/_{512}$	0	LEDs on

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2050 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	SCALE = 1/80	SCALE = 1/160	SCALE = 1/320	SCALE = 1/640	SCALE = 1/1280	SCALE = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh

Therefore:

$$1000\text{mAh} \cdot 0.05\Omega = 50\text{mVh}$$

Select:

PFC = 30720 counts or 48mVh
$PROG_1$ = float
$PROG_2$ = low
$PROG_3$ = high
$PROG_4$ = float
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 48mVh (960mAh) until the bq2050 "learns" a new capacity with a qualified discharge from full to EDV1.

3. **Nominal Available Capacity (NAC):**

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. **Discharge Count Register (DCR):**

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

- No valid charge initiations (charges greater than 256 NAC counts, where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.
- The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
- The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

5. **Scaled Available Energy (SAE):**

SAE is useful in determining the available energy within the battery, and may provide a more useful capacity reference in battery chemistries with sloped voltage profiles during discharge. SAE may be converted to a mWh value using the following formula:

$$E(\text{mWh}) = (SAEH * 256 + SAEL) * \frac{2.4 * SCALE * (R_{B1} + R_{B2})}{Rs * R_{B2}}$$

where R_{B1}, R_{B2} and Rs are resistor values in ohms. SCALE is the selected scale from Table 2. SAEH and SAEL are digital values read via DQ.

6. **Compensated Available Capacity (CAC)**

CAC counts similar to NAC, but contains the available capacity compensated for discharge rate and temperature.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2050 increments NAC at a rate proportional to V_{SR} and, if enabled, activates an LED display. Charge actions increment the NAC after compensation for temperature.

The bq2050 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} (V_{SR} + V_{OS}) falls below V_{SRQ}. V_{SRQ} is 210µV, and is described in the Digital Magnitude Filter section.

Discharge Counting

Discharge activity is detected based on a negative voltage on the V_{SR} input. All discharge counts where $V_{SRO} < V_{SRD}$ cause the NAC register to decrement and the DCR to increment. V_{SRD} is -200µV, and is described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The bq2050 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/512 • NAC per day or disabled. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

Discharge Compensation

Corrections for the rate of discharge, temperature, and anode type are made by adjusting an internal compensation factor. This factor is based on the measured rate of discharge of the battery. Tables 3A and 3B outline the correction factor typically used for graphite anode Li-Ion batteries, and Tables 4A and 4B outline the factors typically used for coke anode Li-Ion batteries. The compensa-

tion factor is applied to CAC and is based on discharge rate and temperature.

Table 3A. Graphite Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
< 0.5C	1.00	100%
≥ 0.5C	1.05	95%

Table 3B.

Temperature	Temperature Compensation Factor	Efficiency
≥ 10°C	1.00	100%
0°C to 10°C	1.10	90%
-10°C to 0°C	1.35	74%
≤ -10°C	2.50	40%

Table 4A. Coke Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
<0.5C	1.00	100%
≥ 0.5C	1.15	86%

Table 4B.

Temperature	Temperature Compensation Factor	Efficiency
≥ 10°C	1.00	100%
0°C to 10°C	1.25	80%
-10°C to 0°C	2.00	50%
≤ -10°C	8.00	12%

Charge Compensation

The bq2050 applies the following temperature compensation to NAC during charge:

Temperature	Temperature Compensation Factor	Efficiency
< 10°C	0.95	95%
≥ 10°C	1.00	100%

This compensation applies to both types of Li-Ion cells.

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/512$ • NAC per day. This is the rate for a battery within the 20–30°C temperature range. This rate varies across 8 ranges from <10°C to >70°C, changing with each higher temperature (approximately 10°C). See Table 5 below:

Table 5. Self-Discharge Compensation

Temperature Range	Typical Rate PROG5 = Z or L
< 10°C	NAC/2048
10–20°C	NAC/1024
20–30°C	NAC/512
30–40°C	NAC/256
40–50°C	NAC/128
50–60°C	NAC/64
60–70°C	NAC/32
> 70°C	NAC/16

Self-discharge may be disabled by connecting $PROG_5$ = H.

Digital Magnitude Filter

The bq2050 has a digital filter to eliminate charge and discharge counting below a set threshold. The bq2050 setting is 200µV for V_{SRD} and 210µV for V_{SRQ}.

Table 6. bq2050 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SRO}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Communicating With the bq2050

The bq2050 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2050 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2050 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends an eight-bit command byte to the bq2050. The command directs the bq2050 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input

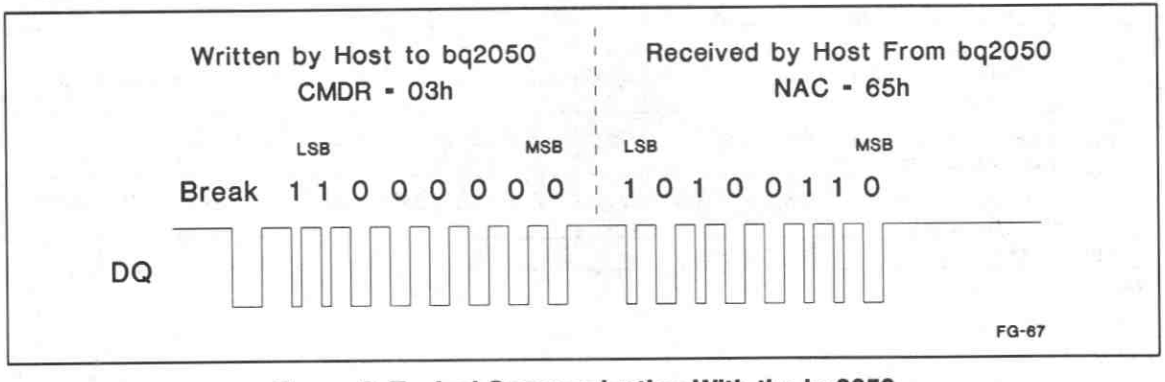


Figure 3. Typical Communication With the bq2050

Table 7. bq2050 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	n/u	CI	VDQ	n/u	EDV1	EDVF
TMP	Temperature register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capacity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	R	n/u	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
VSB	Battery voltage register	0Bh	Read	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0Ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
CACH	Compensated available capacity high byte register	0Dh	R	CACH7	CACH6	CACH5	CACH4	CACH3	CACH2	CACH1	CACH0
CACL	Compensated available capacity low byte register	0Eh	R	CACL7	CACL6	CACL5	CACL4	CACL3	CACL2	CACL1	CACL0
SAEH	Scaled available energy high byte register	0Fh	R/W	SAEH7	SAEH6	SAEH5	SAEH4	SAEH3	SAEH2	SAEH1	SAEH0
SAEL	Scaled available energy low byte register	10h	R/W	SAEL7	SAEL6	SAEL5	SAEL4	SAEL3	SAEL2	SAEL1	SAEL0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

from the bq2050 may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs, e.g. t_{CYCB} > 6ms, the bq2050 should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2050 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2050 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2050 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2050 is always performed with the least-significant bit being transmitted first. Figure 3 on page 9 shows an example of a communication sequence to read the bq2050 NAC register.

bq2050 Registers

The bq2050 command and status registers are listed in Table 7 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2050. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2050 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2050 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the bq2050 is reset either by application of V_{CC} or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 bq2050 is reset

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2050 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2050 is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2050 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register on this page).

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that the discharge rate is < 2C

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery. The EDVF threshold is set 50mV below the EDV1 threshold.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq (V_{TS} - 50mV)$

1 $V_{SB} < (V_{TS} - 50mV)$ providing the discharge rate is < 2C

Temperature Register (TMP)

The read-only TMP register (address=02h) contains the battery temperature.

TMP Temperature Bits							
7	6	5	4	3	2	1	0
TMP4	TMP3	TMP2	TMP1	-	-	-	-

The bq2050 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 7.

Table 7. Temperature Register

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2050 calculates the gas gauge bits, GG3-GG0 as a function of CACH and LMD. The results of the calculation give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2050. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2050 gas gauge operation. Do not write the NAC registers to a value greater than LMD.

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2050. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2050 uses as a measured full reference. The bq2050 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2050 updates the capacity of the battery. LMD is set to PFC during a bq2050 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2010 flags.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	Discharge Rate
0	0	0	DRATE < 0.5C
0	0	1	0.5C ≤ DRATE < 2C
0	1	0	DRATE ≥ 2C (OVLD = 1)

The ***overload*** flag (OVLD) is asserted when a discharge rate in excess of 2C is detected. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after the rate drops below 2C. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2050. The segment drivers, SEG_{1-6}, have a corresponding PPD register location, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2050. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2050 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 • LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 • LMC. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Battery Voltage Register (VSB)

The read-only battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register (address = 0Bh) is updated approximately once per second with the present value of the battery voltage. $V_{SB} = 2.4V \bullet (VSB/256)$.

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The read/write VTS register sets the EDV1 trip point. EDVF is set 50mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 1.52V and EDVF = 1.47V. EDV1 = 2.4V • (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Compensated Available Charge Registers (CACH/CACL)

The read-only CACH high-byte register (address = 0Dh) and the read-only CACL low-byte register (address = 0Eh) represent the available charge compensated for discharge rate and temperature. CACH and CACL use piece-wise corrections as outlined in Tables 3A, 3B, 4A, and 4B, and will vary as conditions change. The NAC and LMD registers are not affected by the discharge rate and temperature.

Scaled Available Energy Registers (SAEH/SAEL)

The read-only SAEH high-byte register (address = 0Fh) and the read only SAEL low-byte register (address = 10h) are used to scale battery voltage and CAC to a value which can be translated to watt-hours remaining under the present conditions. SAEL and SAEH may be converted to mWh using the formula on page 7.

Reset Register (RST)

The reset register (address = 39h) provides the means to perform a software-controlled reset of the device. A device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed,*** *and results in improper operation of the bq2050.*

Resetting the bq2050 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: NACH = PFC at reset when $PROG_6$ = H

Display

The bq2050 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2050 displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the CACH and CACL register descriptions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2050 detects a charge in progress $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active for a period of four seconds, ± 0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2050 can operate directly from 1 cell. A micropower source for the bq2050 can be inexpensively built using the FET and an external resistor to accommodate a greater number of cells; see Figure 1.

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Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2050 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (T_A = T_{OPR}; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	1.45	1.47	1.49	V	SB
V_{EDV1}	First empty warning	1.50	1.52	1.55	V	SB
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	210	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-200	µV	V_{SR} + V_{OS} (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB

Note: V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	2.5	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEGx output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEGx output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCH} = V_{CC} - 0.6V
I_{OLS}	SEG_{1-5} sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_6$

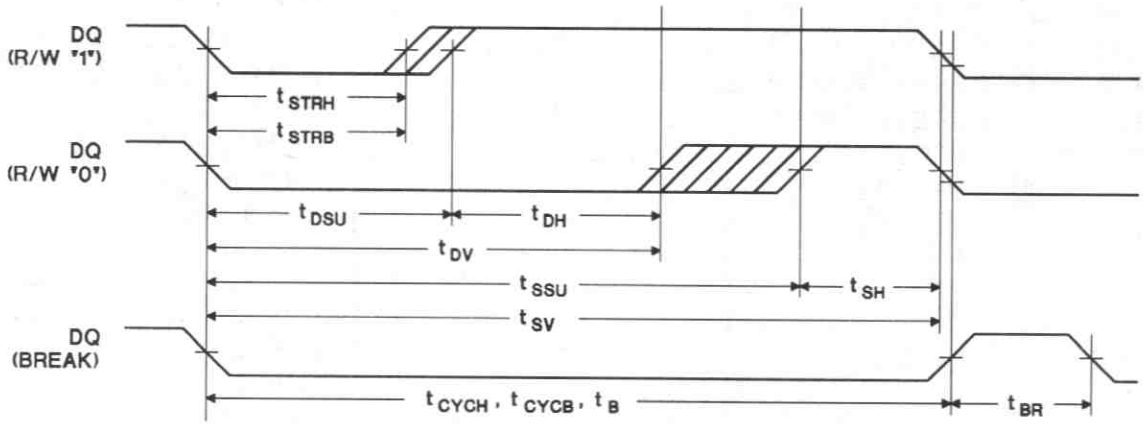
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2050	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2050 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2050	5	-	-	ns	
t_{STRB}	Start hold, bq2050 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



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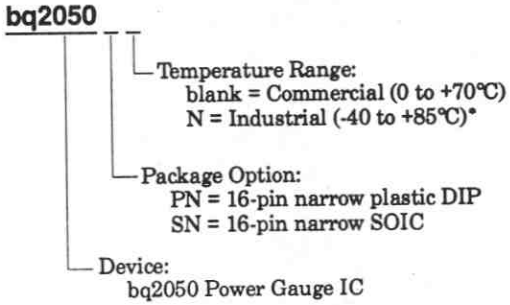
Ordering Information



* Contact factory for availability.

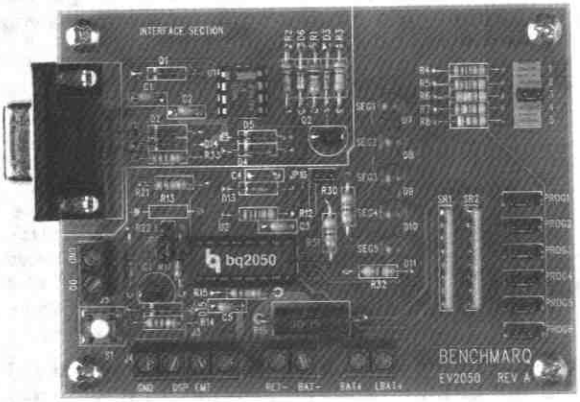
Notes

BENCHMARQ

EV2050

Power Gauge™ Evaluation Board

Contents



Introduction

The bq2050 Power Gauge IC provides battery capacity monitoring in a single 16-pin SOIC or DIP package. The EV2050 Evaluation Board provides a useful means to test bq2050 functionality and easily interface with the device over the RS-232 port of a PC. The bq2050 features:

- Battery capacity monitoring functions
- LED display of available charge
- DQ serial I/O port communications functions

Functional Description

The EV2050 provides functional evaluation of the bq2050 IC on a PCB. The actual implementation of a bq2050-based design will be significantly smaller in size. See the bq2050 data sheet for bq2050 specifications.

Power Source

The bq2050 derives its Vcc from either an external source or from the battery connected to the BAT+ (J1) and BAT– (J2) terminal blocks. Refer to Table 4 in *Using the bq2010—A Tutorial for Gas Gauging* for the proper size of R17 as part of the Vcc regulation. The EV2050 Evaluation Board is shipped with a 200KΩ resistor for R17.

Current Path

The bq2050 uses a sense resistor (R16) on the negative terminal of the battery to measure charge and discharge of the battery. This resistor may be changed if necessary. The system load is connected between the BAT+ (J1) and RET– (J2) terminal blocks (see the schematic in Appendix C).

Parameter Programming

The EV2050 is programmed by the segment programming pins, using jumpers PROG1–PROG5. The programming pins determine:

- Programmed full count
- Scale factor
- Discharge compensation factor
- Self-discharge compensation (on/off)

EV2050 Contents

Each package contains the following items:

1 EV2050 PC Board

This includes the bq2050 sample, current regulator, programming jumpers, battery divider resistors, and the PC serial port interface.

1 EV2050 DQ/RS-232 Cable

1 EV2050 (v2.5) User Interface Program Diskette

This program runs on *any AT-compatible computer* equipped with a standard RS-232 (COM1, COM2, COM3, or COM4) serial port, and provides the user with a complete menu-driven system to control, monitor, and log data from the EV2050 Evaluation Board. The User Interface Program communicates with the bq2050 over the DQ serial I/O port using the RS-232 interface.

Please check to make sure that all items are present and in good condition. If you have any problems, please contact your Benchmarq representative or call Benchmarq.

EV2050 Connections

The connections for the EV2050 are described below. Please refer to the attached schematic in conjunction with these descriptions.

JP1–JP8 **Battery cell divider.** JP1-JP6 are used to divide the battery voltage by 5 to 10. JP7 and JP8 are user-definable, but are configured for 11 and 12 cells on this board.

JP9 **V_{CC} supply.** This jumper is used to select the V_{CC} supply for the bq2050. When JP9 is near Q2, the supply is taken from the BAT+ input and is regulated by the bq2050 and Q2. When JP9 is near R13, the V_{CC} supply is provided by LBAT+. If V_{CC} is supplied by LBAT+, it must not exceed the specified V_{CC} voltage range in the bq2050 data sheet.

JP10–JP14 **Programming pins 1-5.** These jumpers are used to configure the programming pins. When the jumper is positioned near the PROG# designator, the pins are pulled high. If the jumper is in the other position, the pins are pulled low. If the jumper is removed, the pins are in the high-impedance state. The board is shipped with all pins in the high position. Please refer to the bq2050 data sheet for the proper configuration of $PROG_{1-5}$.

JP16 **LED enable** (LCOM connection). This jumper connects the LCOM pin of the bq2050 to the LEDs. The board is shipped with this jumper enabled.

RBI **Register backup input.** This pin is used to provide backup potential to the bq2050 registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

DSP **Display input** ($\overline{DISP}$ pin). DSP is connected in parallel with the push-button switch S1 provided on the EV2050 board. An external switch configuration can be made using DSP. When the EV2050 is floating and detects charging or discharging, the LED outputs are active to reflect the charge state. When the $\overline{DISP}$ input is pulled low, the LEDs reflect the charge state.

EV2050 Configuration

The EV2050 Evaluation Board may be used with or without the DQ/RS-232 Interface Program. The Evaluation Board should first be configured before connecting the battery or the RS-232 cable.

Step 1 Enabling the LEDs (optional)

JP16 should be installed.

Step 2 Connecting the power supply

The EV2050 can operate from power provided by the battery being monitored or from LBAT+. Set the battery divider (JP1–JP8) to the correct number of battery cells prior to connecting the battery. If the bq2050 will be powered from the battery, connect JP9 closer to Q2. If the bq2050 will be powered from an external supply, connect JP9 closer to R13. **Important: Connect the battery ONLY after setting JP1-JP8 and JP9.**

Step 3 Connecting the RS-232 cable

Connect the cable provided to the serial port of any PC. Please ensure no memory-resident programs use this serial port.

Step 4 Connecting the load

The external load is connected between BAT+ and RET- (J2) on the EV2050. A sense resistor (R16) is in series with the negative terminal of the battery. The EV2050 board is supplied with a 0.1, 1% 3W resistor. Please ensure that the discharge load does not exceed the V_{SR} speci-

fication for the bq2050. R16 may be changed to a different-value resistor.

Installing the User Interface Program

The User Interface Program (named "EV2050") runs on any PC-compatible computer. The program may be run from the disk provided, or it may be installed on any directory on the computer's hard disk. To run the program from the hard disk, simply copy all the files from the disk supplied to the hard disk. All the files should reside in the same directory.

The User Interface Program installs a driver to control the DQ/RS-232 interface. This driver asks which COM port is connected to the EV2050 Evaluation board. If communication is not established with the EV2050 board, the Main Menu does not appear. Please refer to Appendix B (Troubleshooting) if the program does not establish communication with the EV2050.

The EV2050 uses the PC-AT real-time clock to provide the proper bit timing for serial communication with the bq2050. The modem control lines are used as the single-wire serial interface to the bq2050. Any TSR that uses the PC real-time clock affects the operation of the EV2050. For proper operation, the EV2050 should not be operated from a DOS shell program.

If the PC is a notebook or portable type, it may be configured to save battery power by adjusting the clocks according to the activity under way. Configure the notebook to run in "High Performance" mode for reliable communication between the EV2050 and the PC. The EV2050 UIP terminates if communication with the EV2050 board is lost.

Start the User Interface Program as follows:

```
C>EV2050
```

Using the EV2050 Program

EV2050 is a menu-driven program. Almost all of the functions and entries are made by positioning the highlighted cursor on the function desired and pressing the ENTER key, or by typing a value and then pressing the ENTER key.

Key functions are as follows:

ARROW keys	Use the arrow keys to move the highlighted cursor around the screen.
ENTER key	Press the ENTER key to select the value currently being displayed for a parameter, or to perform a function selected by the highlighted cursor.
ESCAPE key	Press the ESCAPE key to escape from any function back to the main menu, or to escape from any parameter value screen back to the menu displaying that parameter.
F3 key	Press the F3 key to display a help file for the selected function or parameter.

Main Menu

The Main Menu appears after the EV2050 program has started. If this menu does not appear, communication with the EV2050 has not been established; please refer to Appendix B (Troubleshooting) if the EV2050 does not display the Main Menu.

The Main Menu shows six functions that may be activated; see Figure 1. Use the cursor keys (arrow keys) to position the highlighted cursor over the function to be activated and press the ENTER key. For help, press the F3 key, and a help note about the function appears. Press the ESCAPE key to exit from the EV2050 program.

The Main Menu functions are as follows:

<Initialize>	Sends a reset command to the bq2050.
<Program>	Activates a screen showing the current program settings for the bq2050.
<Monitor mWh> and <Monitor mAh>	Activates a screen from which the bq2050 activity is monitored on a real-time basis. Capacity is indicated in mWh or mAh depending on the screen selected.
<Data Log>	Allows entering a file name to which bq2050 data will be logged, and the logging period in seconds. When the log is activated, the display changes to the Monitor mAh screen with a bottom display of: Logging Record: xx
<Measure Vos>	This allows the user to determine the apparent offset voltage of the bq2050 under test. A minimum of 6 minutes is required to complete the Vos measurement, which has a resolution of ±0.15mV per 6 minutes.

Monitor Screens

The EV2050 software provides two real-time monitoring screens. One reports available battery capacity in Amp-hours, the other in Watt-hours. See Figures 2 and 3. The program continually updates the monitor screen. As conditions change, the new values are displayed.

Time	Time of day in HH:MM:DD, 24-hour notation.
Empty/Full	This indicates the current value for GG in the TMPGG register of the bq2050. The capacity value is given in 1/16th steps.
Date	Current date in MM/DD/YY notation.
NAC	NAC register values multiplied by the scale value and divided by the sense resistor value to give mAh.
SAE	Scaled available energy expressed in terms of mWh.
LMD	Last Measured Discharge expressed in terms of mAh. This is the 8-bit LMD register value multiplied by the scale value times 256 and divided by the sense resistor to give mAh.
LMDW	Last measured discharge expressed in terms of mWh.
Sense Resistor Value	This is the sense resistor value from the Program Menu.
CAC	Compensated available capacity expressed in terms of mAh. CAC is similar to NAC but compensates for discharge rate and temperature.
Temp Step	This is a display of the active temperature step, which ranges from 0 (for temperatures <-30°C) to 12 for temperatures > 80°C).
Average V_{SR} Current	This is the average battery current.
Time Remaining	During discharge, this is the time remaining at the average current (NAC / Avg. V_{SR} current).
Activity	This indicates the charging/discharging activity occurring with the battery. CHARGE is displayed if the battery is charging, while DISCHARGING is displayed if the battery is being discharged, or if it is idle (no charging taking place). OVERLOAD is displayed if the discharge rate exceeds 2C. Please note that the appearance of CHARGE or DISCHARGE indicators is rate-dependent, and may take some time after the application of a charging current or a discharge load depending on the PFC and scale selected, and the rate of charge or discharge being applied.
Discharge Rate	This is the value of the V_{SR} discharge rate current step as defined in the bq2050 data sheet.
GG Step	This is the lower four bits of the TMPGG register that correspond to the current CAC value relative to LMD. The GG step is reported as a step number from 0 to 15, with step 0 representing available capacity from 0 to 1/16 of full, and 15 representing available capacity from 15/16 full to full.
First EDV	This is the state of the EDV1 flag as programmed in the Program Menu. The default is 1.52V. The EDV1 flag latches ON if V_{SB} drops below the EDV1 threshold value. It remains latched until charging is detected, at which time it is cleared.

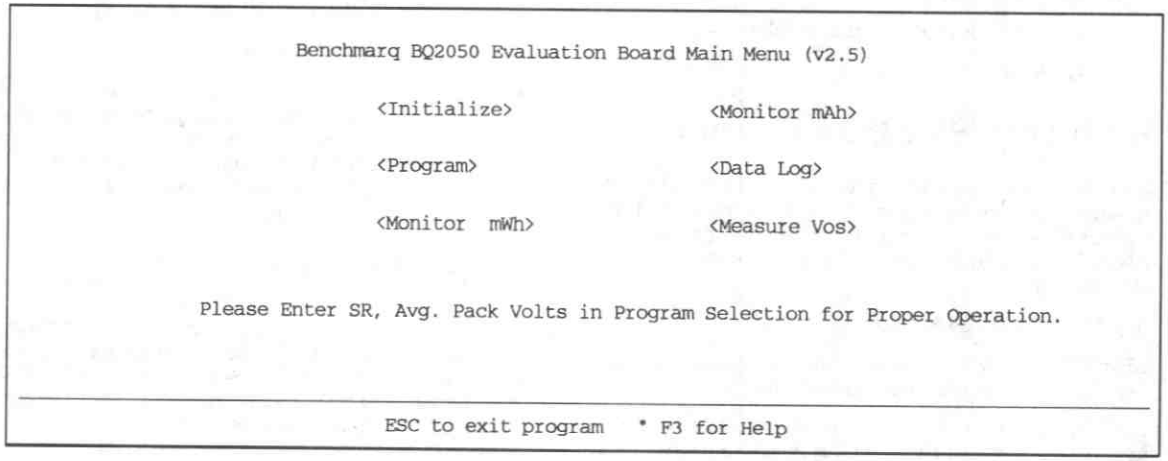


Figure 1. Main Menu

Valid Discharge — This is the state of the VDQ bit in FLGS1. VDQ = yes if the bq2050 is charged until NAC = LMD. VDQ = no indicates the present discharge is not valid for LMD update.

Final EDV — This is the state of the EDVF flag as programmed in the Program Menu. The value of EDVF is set at 1.47V. The EDVF flag latches ON if V_{SB} drops below the EDVF threshold value. It remains latched until charging is detected, at which time it is cleared.

Battery Replaced — This is the state of the battery replaced flag. It is set (BRP = yes) after an EV2050 initialization. The battery replaced flag is cleared if the battery is discharged to the EDV1 level or if it is charged to NAC = LMD.

Pack voltage — This is the cell voltage at the SB pin of the bq2050.

Capacity Inaccurate — This is the state of the capacity inaccurate bit in FLGS1. It is set (CI = yes) to indicate that the battery capacity has not been updated during the last 64 charge cycles.

Capacity Inaccurate Count — This is the number of charge cycles between an LMD update. This counter is reset to zero when NAC = LMD after a valid LMD update.

FLGS1 — This indicates the present state of the FLGS1 register.

FLGS2 — This indicates the present state of the FLGS2 register.

Modifying NAC and LMD

It is possible to change the values of the NAC and LMD parameters from the screen using the F1 and F2 function keys as follows.

```
                    Milli-Amp-Hour Capacity Monitor

      Time: 99:99:99        EMPTY ****_____FULL      Date: 99-99-9999

      NAC: 99999 mAh        LMD:  99999 mAh    Sense Resistor Value: XXXΩ

      CAC: 99999 mAh                           Temp Step: XX

      Avg Vsr Current: ±9999mA                 Time remaining: 9999 min.

      Activity: XXXXX         Vsr Discharge Rate:  XX   GG Step: XX

      Charge Rate: XXXX       First EDV:  XXX
      Valid Discharge: XXX    Final EDV:  XXX          Batt. Replaced: XXX
      Pack Voltage: XXX V
      Capacity Inaccurate: XXX   Capacity Inaccurate Count: XXX

FLGS1: X X _ X X _ X X              FLGS2: _ X X X _ _ _ X
       C B N C V N E E                     N D D D N N N O
       H R / I D / D D                     / R R R / / / V
       G P U   Q U V V                     U 2 1 0 U U U L
       S           1 F                                 D


      ESC to main menu        F1 to modify NAC        F2 to modify LMD
```

Figure 2. Real-Time Monitor Screen (Milli-Amp-Hour)

Changing NAC (F1)

1) Press the F1 key. The NAC field is highlighted.

2) Enter the value in mAh and press the ENTER key to store the value.

Note: Changing NAC disqualifies a subsequent LMD update.

Changing LMD (F2)

1) Press the F2 key. The LMD field is highlighted.

2) Enter the value in mAh and press the ENTER key to store the value.

Data Logging

The data log is activated from the Main Menu by selecting the Data Log function. A filename to be used and the log sample period must be entered. For example:

Log Data to Filename: <filename.ext>
Enter Sample Period (10 sec or greater):<xx>
Opening Data Log File

When the data log is started, the Monitor Screen displays the number of the current log record in the lower right-hand corner. To terminate the data log, press the ESCAPE key. The file is closed and data logging is terminated.

The data log record contains fields of ASCII data separated by tab characters. The field names and descriptions in record order are listed below.

TIME Time record written in seconds

LMD LMD value in mAh

```
                    Milli-Watt-Hour Capacity Monitor

      Time: 99:99:99       EMPTY ****____FULL      Date: 99-99-9999

      SAE: 99999 mWh       LMDW:  99999 mWh   Sense Resistor Value: XXXΩ

      CAC: 99999 mAh                          Temp Step: XX

      Avg Vsr Current: ±9999mA                Time remaining: 9999 min.

      Activity: XXXXX        Vsr Discharge Rate:  XX   GG Step: XX

      Charge Rate: XXXX      First EDV:  XXX
      Valid Discharge: XXX   Final EDV:  XXX          Batt. Replaced: XXX
      Pack Voltage: XXX V
      Capacity Inaccurate: XXX   Capacity Inaccurate Count: XXX

FLGS1: X X _ X X _ X X              FLGS2: _ X X X _ _ _ X
       C B N C V N E E                     N D D D N N N O
       H R / I D / D D                     / R R R / / / V
       G P U   Q U V V                     U 2 1 0 U U U L
       S           1 F                                 D


                              ESC to main menu
```

Figure 3. Real-Time Monitor Screen (Milli-Watt-Hour)

NAC	NAC value in mAh
Avg. Discharge Current	Average V_{SR} battery current
PACK V	Pack voltage
CAC	CAC value in mAh
SAE	SAE value in mWh
LMDW	LMDW value in mWh
FLAGS1	Binary setting of FLAGS1 flags:

Bit	Meaning
0	EDVF flag state
1	EDV1 flag state
2	Not used
3	VDQ (valid discharge)
4	Capacity inaccurate
5	Not used
6	Battery replaced flag state
7	Charge active flag state

FLAGS2 Binary setting of FLAGS2 flags:

Bit	Meaning
0	Overload flag state
1–3	Not used
4–6	Discharge rate
7	Not used

The log records should be readable by most spreadsheet programs.

Program Menu

This menu is accessed by selecting the <Program> function on the Main Menu. The programming menu allows the user to set and observe the program state of the bq2050; see Figure 4. To change the bq2050 PFC programming, reconfigure jumpers JP10–JP14 and initialize the bq2050. The reset allows the bq2050 to read the program pins.

Sense Resistor — Press F1 to enter the value of sense resistor in ohms. Typical values range from 0.02 to 0.1Ω.

The sense resistor value is used by the EV2050 UIP to develop meaningful information in terms of A, mA, mAh, and mWh

```
                    Benchmarq BQ2050 Programming

Sense Resistor:     0.1 Ω          Scale Factor:      1/160

Display Mode:       RELATIVE       PFC Count:   XXXXX
                                   PFC (mVH):   XXXX
Self-Discharge                     Battery Capacity   9999 mAh
Rate:               1/512C/day
Battery Type:                X     1 = Graphite  2 = Coke

 End of Dschg:             X.XX
Avg  Pack V:               X.XX
Divider Ratio:               X
Programming Pin Configuration
  Prog-1  H    Prog-4  L
  Prog-2  Z    Prog-5  L
  Prog-3  Z    Prog-6  Z

F1 = SR  F2 = Bat. Type  F3 = EDV  F4 = PACK  F5 = Div. Ratio  ESC = main
```

Figure 4. Program Menu

	in relation to battery capacity and current. The default value is 0.1. Values from 0.005 to 0.256 are saved in the battery ID RAM byte of the bq2050. Values greater than 0.256 must be re-entered each time EV2050 is started.
Scale Factor	Select the scale factor from the available scales using JP12. Like the sense resistor, the scale factor is used to develop meaningful information for the programmed full count tables, battery full, and available capacity indications.
Display Mode	The RELATIVE display mode uses the last measured discharge capacity of the battery as the battery-full reference.
PFC Count	Program full count from Table 2 from the bq2050 data sheet.
PFC (mVH)	Select the programmed full count using JP10 and JP11. Note that the selected PFC and the sense resistor value are used to determine the initial battery full capacity (mAh) represented by the PFC.
Battery Capacity	This display indicates the battery capacity represented by dividing the PFC by the sense resistor. In practice, picking a PFC and sense resistor that provide a battery full value slightly lower than (within 5%) the rated battery capacity is recommended.
Self-Discharge Rate	Set at 1/512C per day for lithium-ion.
Battery Type	Select coke or graphite anode with J14.
End of Dschg	Press F3 to enter the desired end of discharge voltage for the battery pack. The default value is 1.52V for the bq2050.
Avg Pack V	Press F4 to enter the average pack voltage.
Divider Ratio	Press F5 to adjust the reported pack voltage scaled per the equation in the bq2050 data sheet.
Programming Pin Configuration	This displays indicates the programming of the bq2050 by displaying H, Z, or L depending on the state of the program pins. Please refer to the bq2050 data sheet for further details.

Measure Vos Screen

This screen is used to measure the V_{OS} of the bq2050; see Figure 5. A minimum of 360 seconds is required to perform this test. Pressing the ESC key terminates the test in progress. Operating the test for a longer period increases the resolution of the test. A "beep" signals test completion.

```
                Benchmarq EV2050 Evaluation Board Vos Measurement

Present DMF Setting          -XXXmV=Vsrd      +XXXmV=Vsrq
Current Threshold (DMF(mv)/Rsns): XXXXmA
Do you want to test Vos?:  Y/N
Calculated Vos:  Vos  XXXmV, over last xxxx seconds
Elapsed time:  XXXX seconds

**Note:  There must be no charge/discharge activity on the bq2050 for this test
         to be valid.  Running the test for a longer period of time increases
         the Vos measurement resolution.  This test requires a minimum
         of 6 minutes before any value is displayed.

                              ESC to main menu
```

Figure 5. Vos Measurement Screen

Appendix A: AP50A User's Guide

The AP50 utility (AP50A.EXE) is used to communicate with the bq2050 on a register basis. AP50 uses a driver to communicate with the EV2050 over serial port on a PC-AT personal computer.

AP50

The AP50 utility is started by executing AP50A.EXE. After AP50 is started, the following prompt is displayed:

Select COM Port < 1 2 3 4 >

Commands

The user can respond with various commands at the prompt. Pressing "Q" causes the program to terminate.

-> ?

Pressing the ? key displays following menu:

```
The following commands are available:
    ?          This display is shown.
    A          Send break.
    Q          Quit and return to DOS.
    R##        Read at Address ##.
    S##        Scan at Address ##.
    W##-**     Write at Address ## value **.
```

These commands may be used to send or receive data from the EV2050.

-> A

If A is entered in response to ->, then a break bit is sent to the EV2050. This may be used to restart the communication if a problem appears. If the prompt does not return immediately, then proper communication has not been established; please refer to Appendix B for troubleshooting procedures.

-> R##

If R## is entered in response to ->, where ## is an applicable address in HEX format, AP50 returns the value at that location from the EV2050. The addresses are defined in the bq2050 data sheet. For example:

-> R03

causes the display to show:

R03= ##

where ## is the current NAC value in HEX format.

Address 00 is used to read and display all readable registers.

-> S##

If S## is entered in response to ->, where ## is a valid bq2050 address in HEX format, AP50 continuously reads and displays the value at that location. The addressed are defined in the bq2050 data sheet. For example:

-> S03

causes the display to show:

Address 3 = ## after XXX.XX sec.

where ## is the value at location 03 and XXX.XX is the number of seconds between changes in this value. Press ESC to return to the prompt.

-> W## = **

If W##=** is entered in response to ->, where ## is an applicable address in HEX format and ** is the value to be written, AP50 writes the value to that location. The addresses are defined in the bq2050 data sheet. For example:

-> W05 = A0

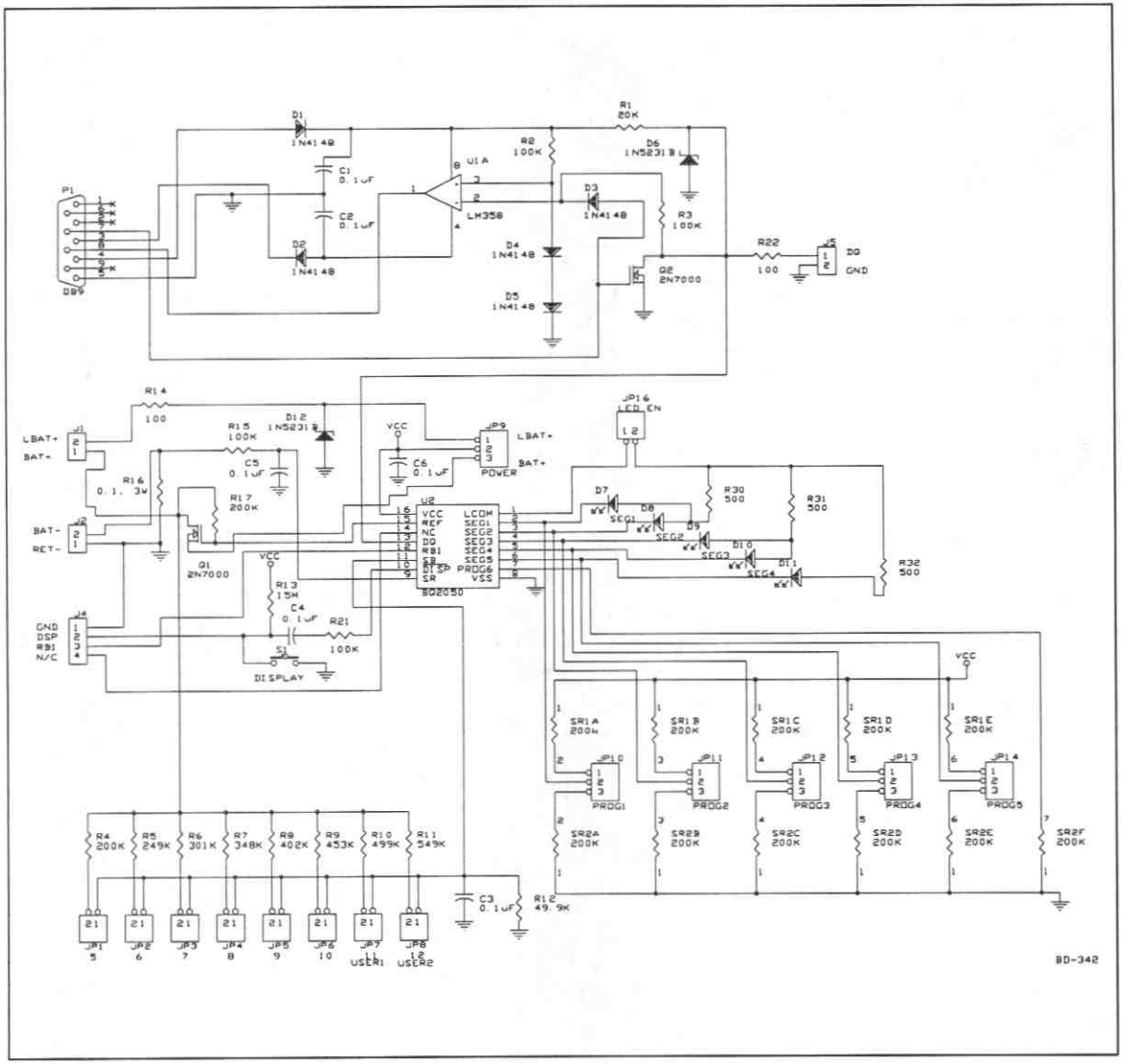
causes the program to write A0 in location 05hex (LMD register).

Appendix B: Troubleshooting

If the EV2050 Main Menu does not appear after starting EV2050, then communication to the bq2050 has not been established. Please check the following:

1. Confirm the proper serial port is being used.
2. Confirm the battery divider is properly set for the number of cells in the battery pack.
3. Confirm JP9 is properly set for either an external supply through LBAT+ (J1) or the microregulator. JP9 closer to Q2 enables the microregulator, while JP9 closer to R13 enables LBAT+. If the battery divider on JP9 is not set properly, the bq2050 will not operate, and the EV2050 UIP or AP50 will not work.
4. Confirm the battery is attached between BAT+ and BAT– (J1 and J2).
5. Push S1. SEG1 LED should be on indicating that the bq2050 is properly powered.
6. If the LED is not on, check the battery voltage on pin 16 of the bq2050 to determine if it is above 3V but below 6.5V.
7. If the LED is on, and the EV2050 Main Menu still does not appear, try using AP50 to establish communication. Appendix A describes AP50.
8. If communication cannot be established using AP50, the problem is either the RS-232 port in the PC or the EV2050 interface section. Please contact Benchmarq if the interface section is not working properly on the EV2050 board.

Appendix C: EV2050 Schematic



Lithium Ion Pack Supervisor

Features

- Protects two to four Lithium Ion series cells from overvoltage, undervoltage, and short circuit
- Designed for battery pack integration
  - Small outline package, minimal external components and space, and low cost
  - Drives external N-FET switches
- User selectable threshold mask programmable by Benchmarq
- Operates on very low current, < 15 µA
- Operates on very low standby current, < 1µA
- Available in 8-pin 150-mil SOIC and 300-mil DIP

General Description

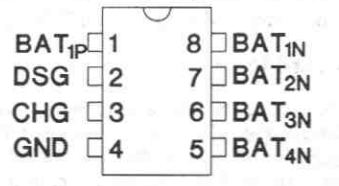
The bq2053 Lithium Ion Pack Supervisor is designed to control the charge and discharge voltage safety limits for two to four lithium ion (Li-Ion) series cells, accommodating battery packs containing series/parallel configurations. The very low operating current does not overdischarge the cells during periods of storage, and does not significantly increase the system discharge load. The bq2053 can be part of a low-cost Li-Ion charge control system within the battery pack.

The bq2053 controls two external N-FETs to limit the charge and discharge potentials. Charging is allowed when the per cell voltage is below V_{CE} (charge enable voltage). When the cell voltage on any cell rises above V_{OV} (overvoltage limit), the CHG pin goes low, shutting off the charge to the battery pack. This safety feature prevents overcharge on any individual series cell stack within the battery pack.

Discharge is allowed when the per-cell voltage is above V_{UV} (undervoltage limit). If the voltage across any cell falls below V_{UV} (undervoltage limit), both the DSG and CHG outputs go low, shutting off the battery discharge. This safety feature prevents overdischarge on any individual series cell stack within the battery pack.

V_{UV}, V_{CE}, and V_{OV} are programmed at Benchmarq. The default limits are 2.3V, 4.15V, and 4.25V, respectively.

Pin Connections



8-Pin Narrow DIP or SOIC

PN-86

Pin Names

BAT_{1P}	Battery 1 positive input
BAT_{1N}	Battery 1 negative input
BAT_{2N}	Battery 2 negative input
BAT_{3N}	Battery 3 negative input
BAT_{4N}	Battery 4 negative input
DSG	Discharge control
CHG	Charge control
GND	Ground

Pin Descriptions

BAT_{1P} **Battery 1 positive input**

This input is connected to the positive terminal of the cell designated BAT_1 in Figure 2.

BAT_{1N} **Battery 1 negative input**

This input is connected to the negative terminal of the cell designated BAT_1 in Figure 2. This input is connected to BAT_{1P} for less than four cells in a series.

BAT_{2N} **Battery 2 negative input**

This input is connected to the negative terminal of the cell designated BAT_2 in Figure 2. This input is connected to BAT_{1P} and BAT_{1N} for less than three cells in a series.

BAT_{3N} **Battery 3 negative input**

This input is connected to the negative terminal of the cell designated BAT_3 in Figure 2.

BAT_{4N} **Battery 4 negative input**

This input is connected to the negative terminal of the cell designated BAT_4 in Figure 2.

CHG **Charge control output**

This output controls the charge path to the battery pack. When this output is high, charging is allowed.

DSG **Discharge control output**

This output controls the discharge path to the battery pack. When this output is high, discharge is allowed.

GND **System Ground**

Battery pack return.

Functional Description

Figure 1 is a block diagram outlining the major components of the bq2053. Figure 2 shows a typical application example. The various functional aspects of the bq2053 are detailed in the following sections.

Configuration

The bq2053 may be configured to supervise two-, three-, or four-series cell packs. For two-series cell configurations, BAT_{1N} and BAT_{2N} are connected to BAT_{1P}. For three-series cell configurations, BAT_{1N} is connected to BAT_{1P}. The bq2053 controls two external N-FETs connected for low side control of the battery pack.

Thresholds

The bq2053 monitors three thresholds for overcharge and overdischarge protection. These thresholds are programmed at Benchmarq. The default values are:

V_{OV} = 4.25 ± 1.5% (overvoltage during charge)

V_{CE} = V_{OV} – 100mV ± 50mV (charge enable voltage)

V_{UV} = 2.3V ± 100mV (undervoltage during discharge)

Please contact Benchmarq for other voltage options.

Charge Supervision

Overvoltage protection is asserted when any of the cell voltages exceed the V_{OV} threshold. Once V_{OV} is reached, the CHG pin is connected to GND, disabling charge into the battery pack. This condition continues until all cell voltages fall below V_{CE}. This indicates that the overcharge has stopped and the pack is ready to accept further charge. When this occurs, CHG and DSG are connected internally to BAT_{1P}, turning on the control FETs until the next time an overvoltage condition is reached.

Discharge Supervision

Overdischarge protection is asserted when any of the cell voltages fall below the V_{UV} threshold. Once V_{UV} is reached, DSG is connected to BAT_{4N} and CHG to GND, disabling the discharge of the pack. This condition continues until GND falls below BAT_{4N} indicating that the overdischarge has stopped, and the pack is now connected to a charging source.

Over-Current Supervision

Over-current protection is asserted when the bq2053 determines that the pack is shorted during constant voltage charge or during discharge. If a voltage greater than ±250mV is detected between BAT_{4N} and GND, CHG will be connected to GND and DSG to BAT_{4N}.

Low-Power Mode

The bq2053 operating current is less than 1µA in the over-discharge operating mode, and less than 15µA in normal operation. This avoids possible cell damage due to overdischarging the battery pack, and extends the storage time between recharge.

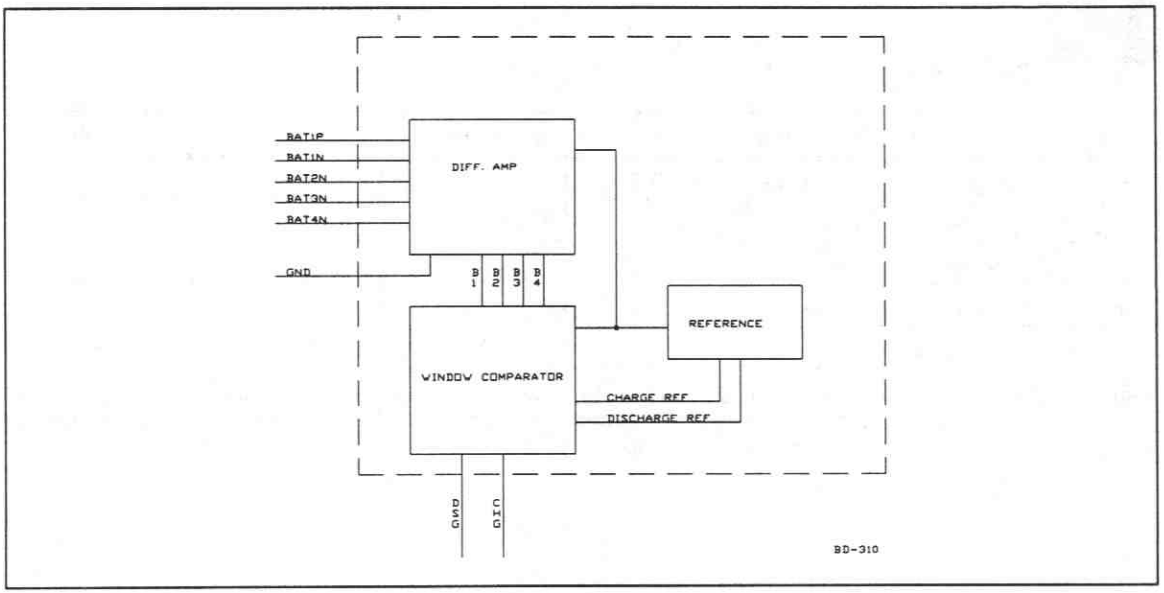


Figure 1. Block Diagram

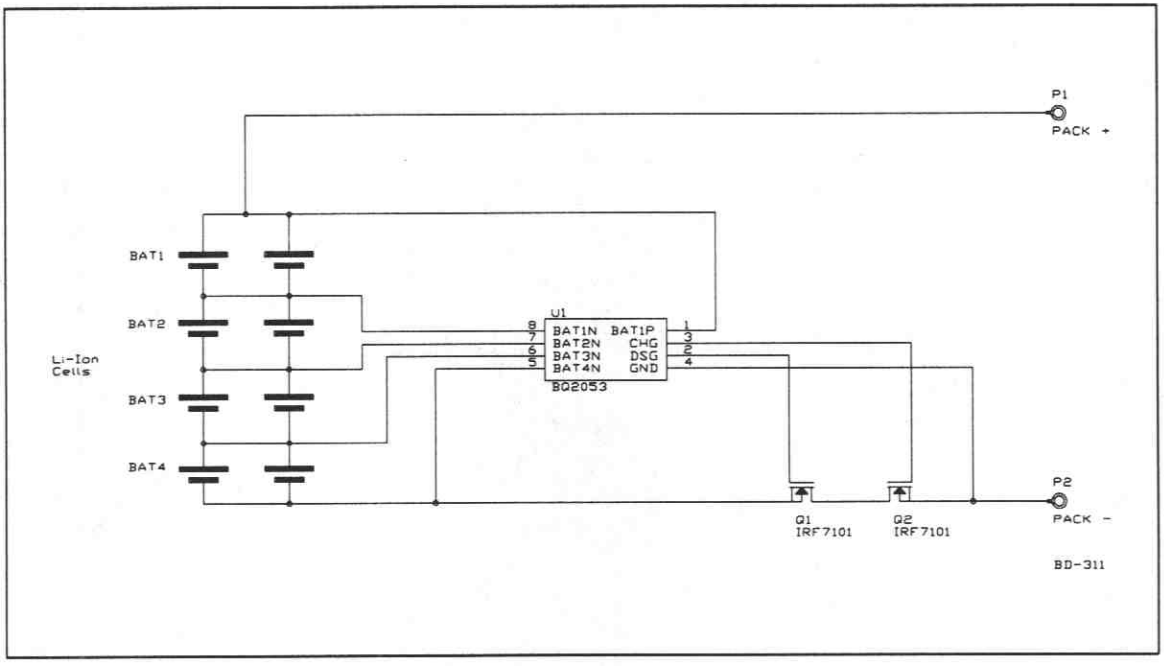


Figure 2. Application Diagram: 4x2 Cell Configuration

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_T	Voltage applied on any pin relative to BAT_{1P}	-18 to +0.31	V	
T_{OPR}	Operating temperature	-30 to +85	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics (T_A = T_{OPR})

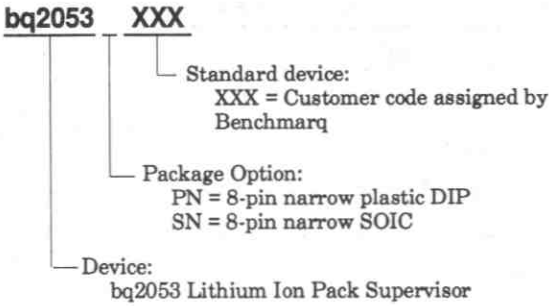
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OH}	Output high voltage	BAT_{1P} - 0.1	-	-	V	I_{OH} = 100 µA, CHG, DSG
V_{OL}	Output low voltage	-	-	BAT_{4N} +0.5	V	I_{OL} = 100 µA, DSG
		-	-	GND + .05	V	I_{OL} = 100 µA, CHG
I_{CC}	Operating current	-	-	15	µA	
I_{CCLP}	Low power current			1	µA	

DC Thresholds (T_A = T_{OPR})

Symbol	Parameter	Value	Tolerance	Unit
V_{OV}	Overvoltage limit	4.25	± 1.5%	V
V_{CE}	Charge enable voltage	V_{OV} - 100mV	± 50mV	V
V_{UV}	Undervoltage limit	2.3	± 100mV	V
V_{CH}	Re-enable CHG or DSG, overcurrent limit	± 250	± 50	mV

Note: Standard device. Contact Benchmarq for different threshold options.

Ordering Information



Preliminary bq2110

Gas Gauge Module

Features

- Complete bq2010 Gas Gauge solution for NiCd or NiMH battery packs
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring customized for 3- to 12-cell series applications (contact Benchmarq for greater than 12 cells)
- On-board regulator allows direct connection to the battery
- Contacts for 6 LED outputs for state-of-charge information display
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration

General Description

The bq2110 Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCD and NiMH battery packs. Designed for battery pack integration, the bq2110 incorporates a bq2010 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor the capacity of 3- to 12 series cells. Contacts are provided on the bq2110 for direct connection to the battery stack (BAT+, BAT-), six LEDs, the serial communications port (DQ), the empty indicator (EMPTY) and the display control input ($\overline{DISP}$). Please refer to the bq2010 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2110 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode. Please contact Benchmarq for gas gauging solutions for other battery chemistries or pack configurations greater than 12 series cells.

The onboard sense resistor accurately measures the charge and discharge activity of the battery pack. The resistor value and type should be specified on the configuration sheet. To minimize module height, a surface mount (SMD) sense resistor can be selected. Refer to page 4 for the bq2110 physical dimensions.

A module development kit is also available for the bq2110. The bq2110B-KT includes one configured module and the following:

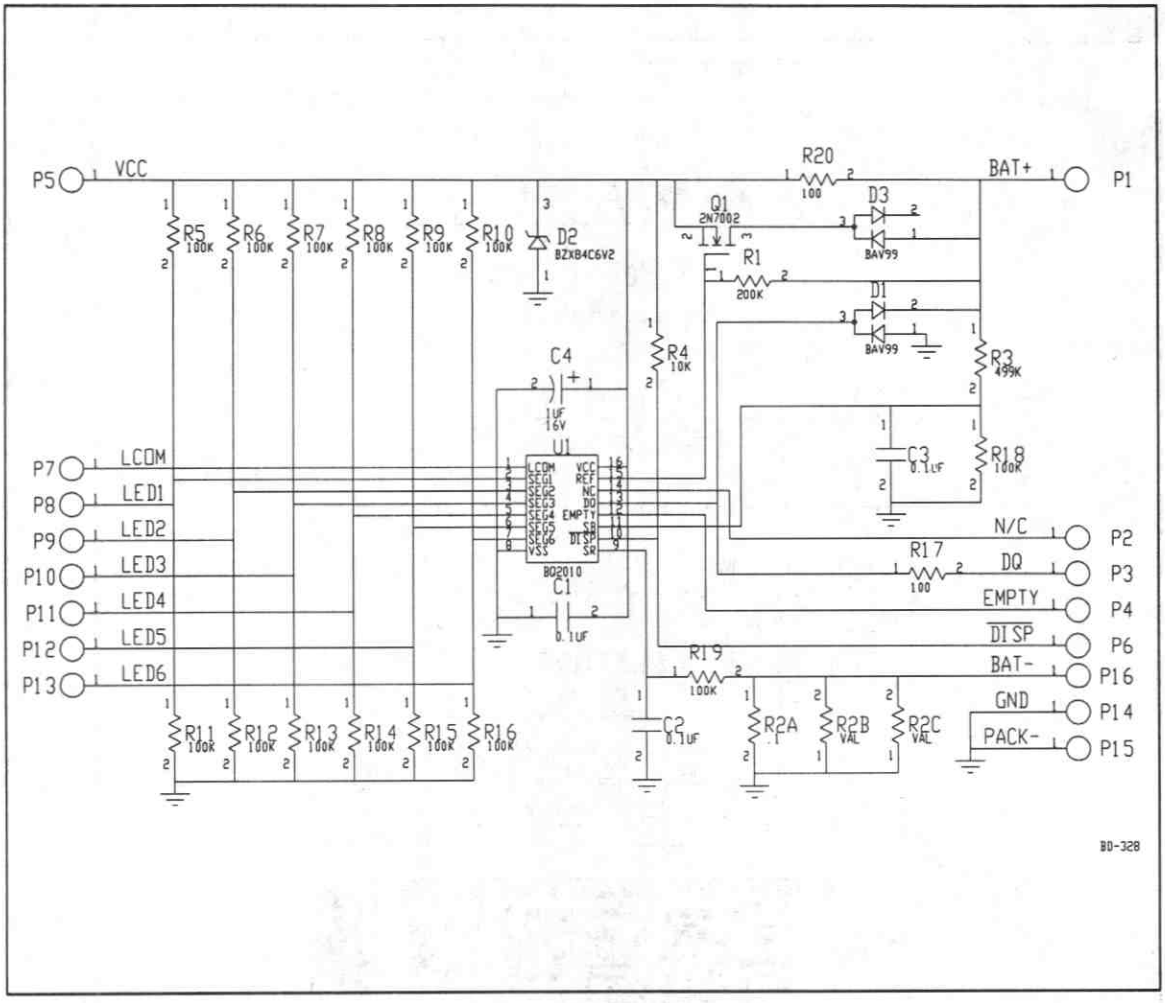
1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2110 to display charge/discharge activity and to allow user interface to the bq2010 from any standard DOS PC.
3) Source code for the TSR.

Table 1. bq2110 Module Configuration

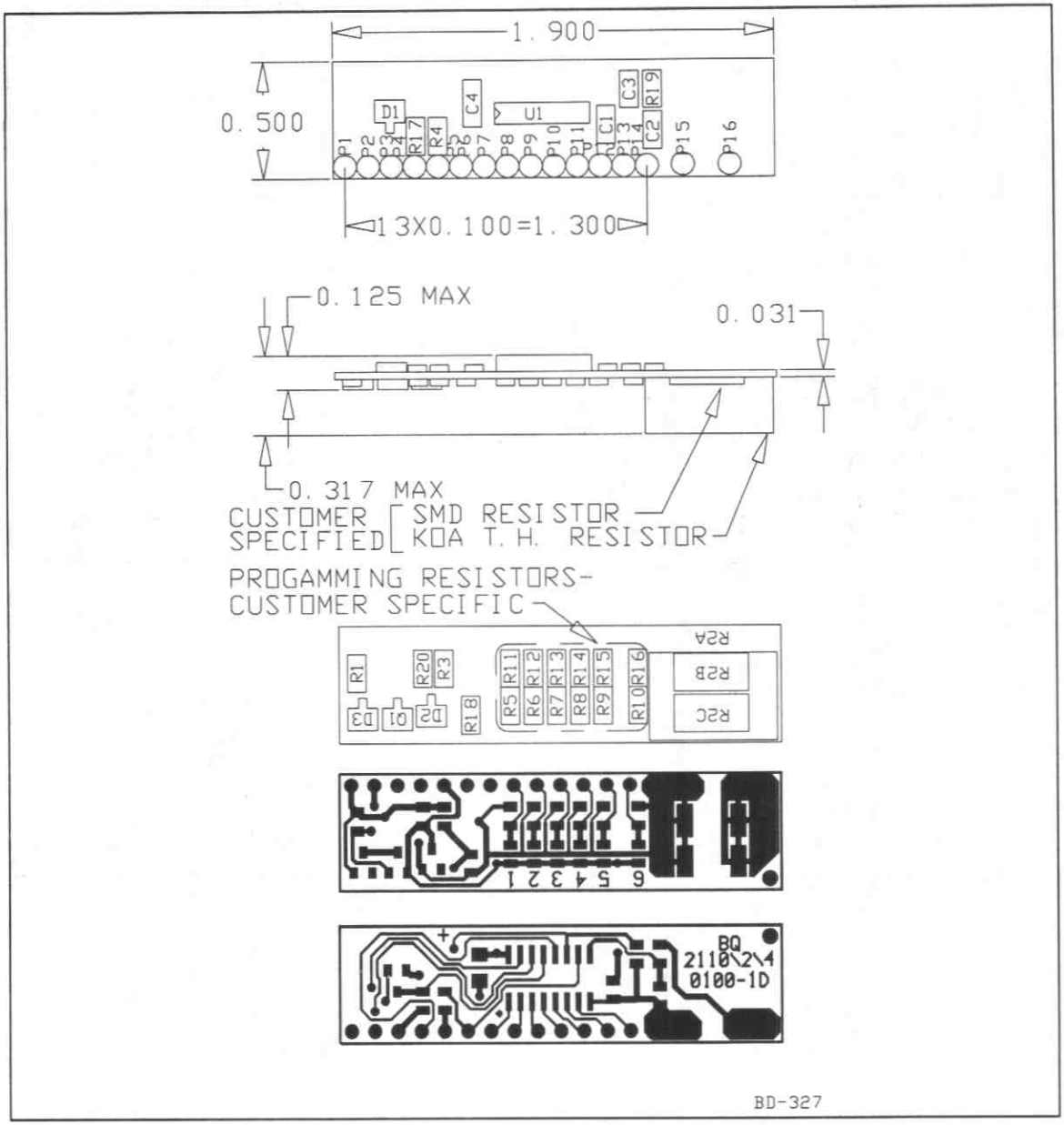
Customer Name:	
Contact:	Phone:
Address:	
Sales Contact:	Phone:
Number of series battery cells (3–12)	
Sense resistor size in mΩ (0.1Ω standard)	
Sense resistor type: KOA(2W), SMD(1W), 2xSMD(1W)	
Battery pack capacity (mAh)	
Battery type (NiCd or NiMH)	
Display mode (absolute or relative)	

Comments:

bq2110 Example Schematic



bq2110 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to Vss	-0.3	+7.0	V	
All other pins	Relative to Vss	-0.3	+7.0	V	
P_{SR}	Continuous sense resistor power dissipation	-	2	W	KOA sense resistor
		-	2	W	2 SMT sense resistors in parallel
		-	1	W	SMT sense resistor
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V_{CC} = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB, BAT+/NumCell
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB, BAT+/NumCell
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, V_{SR} + V_{OS}
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	375	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-300	µV	V_{SR} + V_{OS} (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB, BAT+/NumCell
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Note: Default value; value set in DMF register.

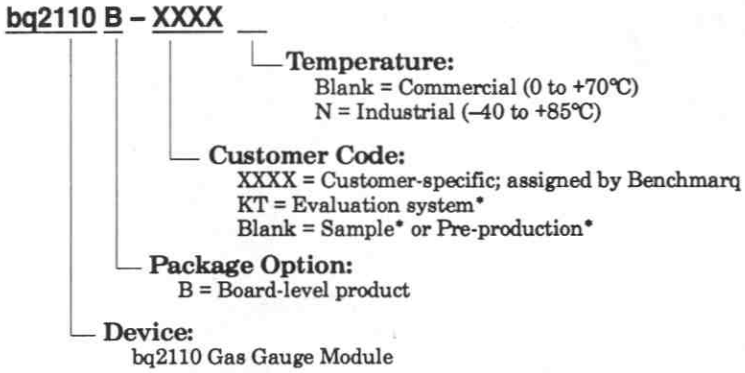
DC Electrical Characteristics (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
NumCell	Number of series cells in battery pack	3	-	12	-
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V
V_{CC}	Supply voltage, 0.93 * NumCell < BAT+ < 1.8 * NumCell[2]	3.0	4.25	6.5	V
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]
R_{DISP}	Pull-up	-	10K	-	Ω
V_{OLSL}	SEGx output low, V_{CC} = 3.0, I_{OLS} < 1.75mA	-	0.1	-	V[1]
V_{OLSH}	SEGx output low, V_{CC} = 6.5, I_{OLS} < 1.75mA	-	0.4	-	V[1]
V_{OHLCL}	LCOM output high, V_{CC} = 3.0, I_{OHLCOM} - -5.25mA	V_{CC} - 0.3	-	-	V[1]
V_{OHLCH}	LCOM output high, V_{CC} = 6.5, I_{OHLCOM} - -33.0mA	V_{CC} - 0.6	-	-	V[1]
I_{OHLCOM}	LCOM source current	-33.0	-	-	mA[1]
I_{OLS}	SEGx sink current	-	-	11.0	mA[1]
I_{OL}	Open-drain sink current DQ, EMPTY	-	-	5.0	mA[1]
V_{OL}	Open-drain output low, I_{OL} < 5mA, DQ, EMPTY	-	-	0.5	V[1]
V_{IHDQ}	DQ input high	2.5	-	-	V[1]
V_{IHDQ}	DQ input low	-	-	0.8	V[1]
V_{OS}	Voltage offset			150	µV[1]

Notes: 1. Characterized on PCB, IC 100% tested.

2. Except in a 3-cell configuration, where 1.0 * NumCell < BAT+ < 1.8 * NumCell.

Ordering Information



*Requires configuration sheet (see Table 1)

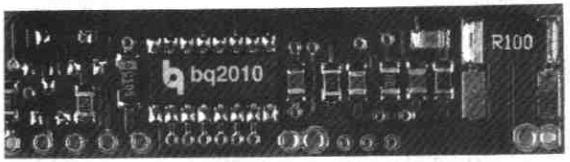
Notes

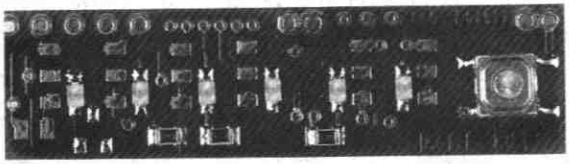
Preliminary bq2110L

Gas Gauge Module with LEDs

Features

- Complete bq2010 Gas Gauge solution for NiCd or NiMH battery packs
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring customized for 3- to 12-cell series applications (contact Benchmarq for greater than 12 cells)
- On-board regulator allows direct connection to the battery
- 6 surface-mounted LEDs to display state-of-charge information
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration





General Description

The bq2110L Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCD and NiMH battery packs. Designed for battery pack integration, the bq2110L incorporates a bq2010 Gas Gauge IC, a current sense resistor, six surface-mounted LEDs, and all other components necessary to accurately monitor and display the capacity of 3- to 12 series cells. Contacts are provided on the bq2110L for direct connection to the battery stack (BAT+, BAT-), the serial communications port (DQ), and the empty indicator (EMPTY). Please refer to the bq2010 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2110L based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode. Please contact Benchmarq for gas gauging solutions for other battery chemistries or pack configurations greater than 12 series cells.

The onboard sense resistor accurately measures the charge and discharge activity of the battery pack. The resistor value and type should be specified on the configuration sheet. To minimize module height, a surface mount (SMD) sense resistor can be selected. Refer to page 4 for the bq2110L physical dimensions.

A module development kit is also available for the bq2110L. The bq2110LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2110L to display charge/discharge activity and to allow user interface to the bq2010 from any standard DOS PC.
3) Source code for the TSR.

Table 1. bq2110L Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

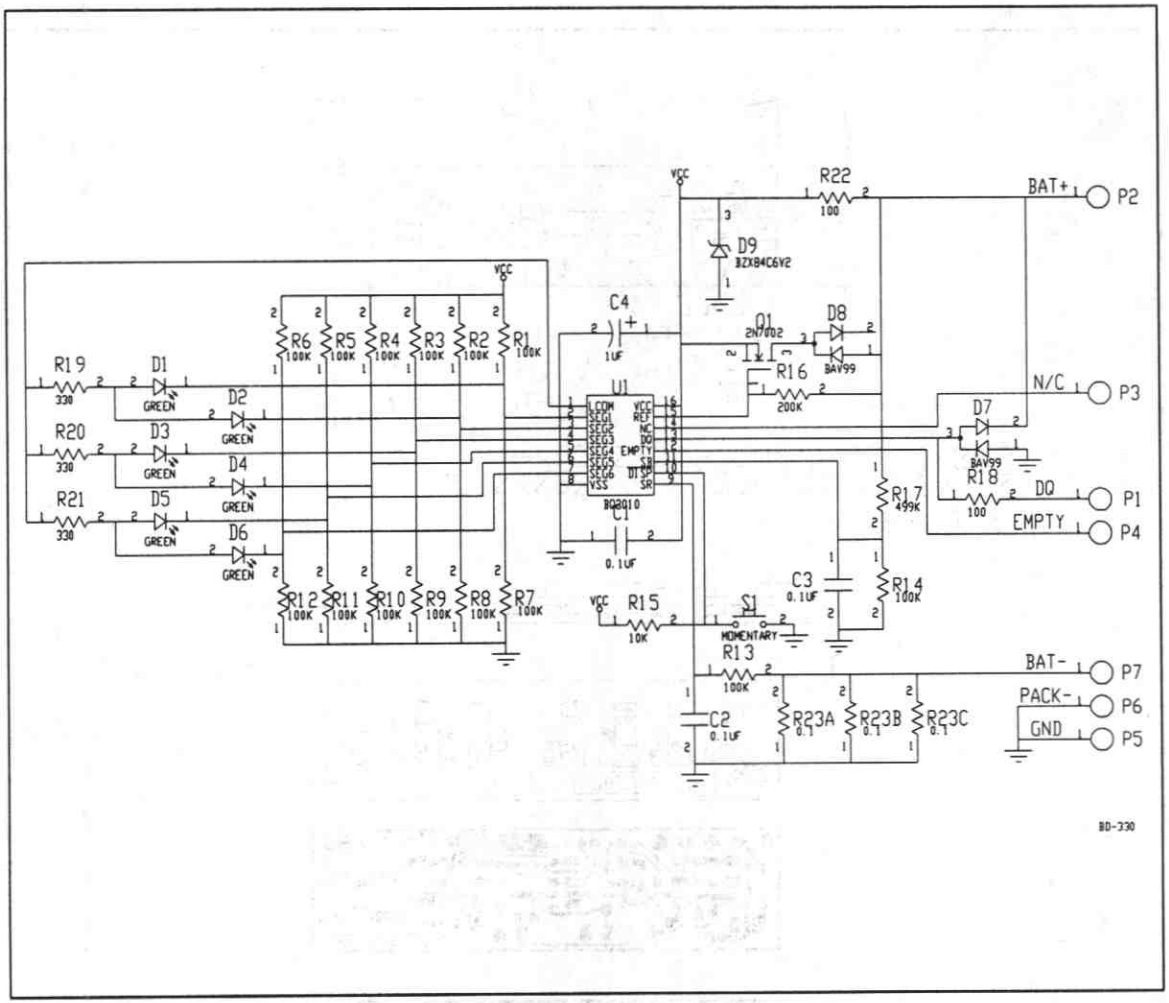
_____

Sales Contact: _____ Phone: _____

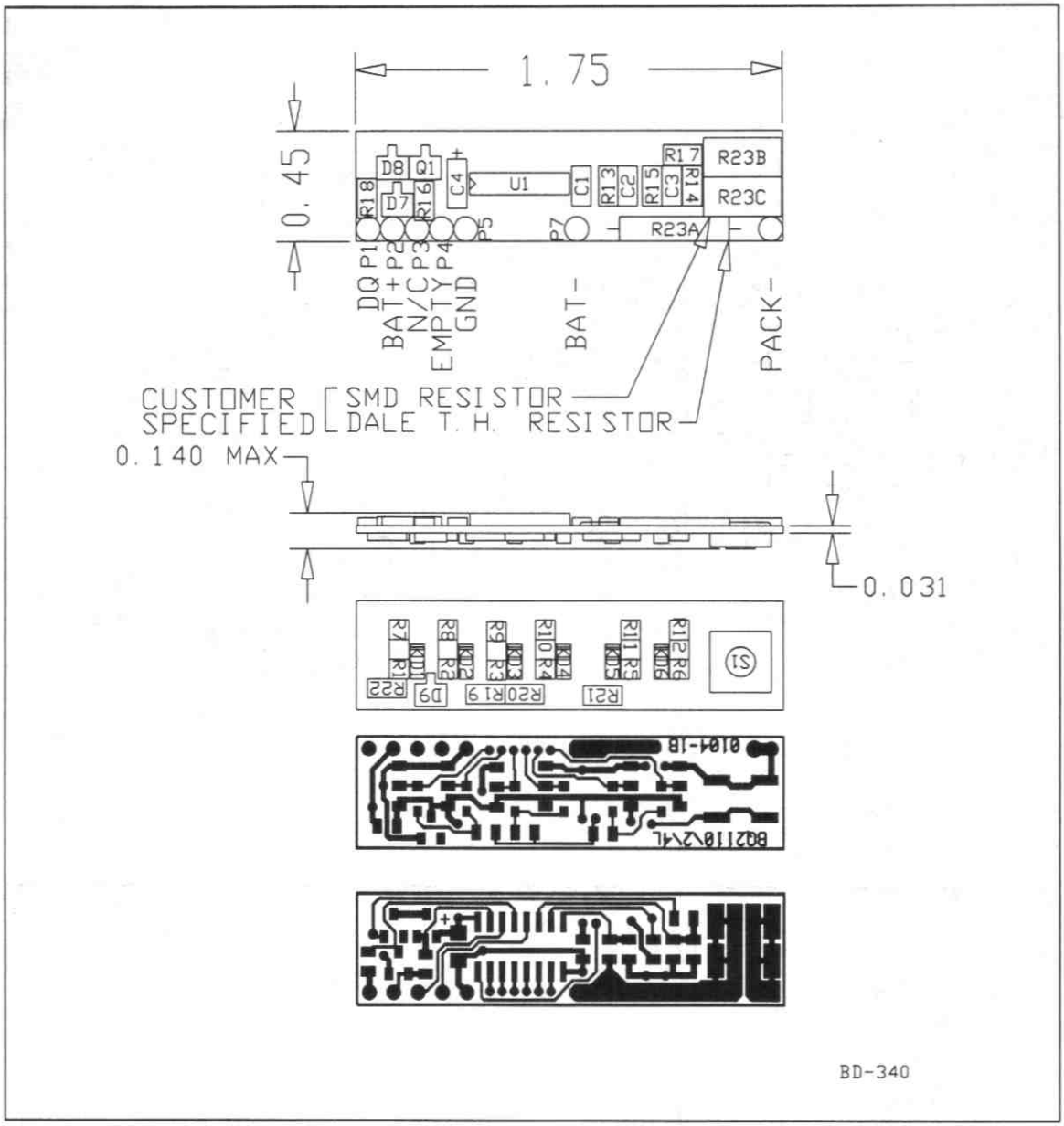
Number of series battery cells (3–12)	_____
Sense resistor size in mΩ (0.1Ω standard)	_____
Sense resistor type: DALE(3W), SMD(1W), 2xSMD(1W)	_____
Battery pack capacity (mAh)	_____
Battery type (NiCd or NiMH)	_____
Display mode (absolute or relative)	_____

Comments:

bq2110L Example Schematic



bq2110L Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
P_{SR}	Continuous sense resistor power dissipation	-	3	W	DALE sense resistor
		-	2	W	2 SMT sense resistors in parallel
		-	1	W	SMT sense resistor
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (T_A = T_{OPR}; V_{CC} = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB, BAT+/NumCell
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB, BAT+/NumCell
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, V_{SR} + V_{OS}
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	375	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-300	µV	V_{SR} + V_{OS} (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB, BAT+/NumCell
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Note: Default value; value set in DMF register.

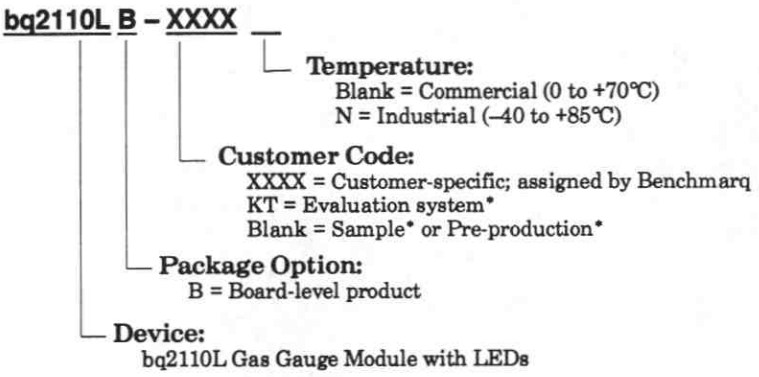
DC Electrical Characteristics (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
NumCell	Number of series cells in battery pack	3	-	12	-
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V
V_{CC}	Supply voltage, 0.93 * NumCell < BAT+ < 1.8 * NumCell[2]	3.0	4.25	6.5	V
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]
I_{OL}	Open-drain sink current DQ, EMPTY	-	-	5.0	mA[1]
V_{OL}	Open-drain output low, I_{OL} < 5mA, DQ, EMPTY	-	-	0.5	V[1]
V_{IHDQ}	DQ input high	2.5	-	-	V[1]
V_{ILDQ}	DQ input low	-	-	0.8	V[1]
V_{OS}	Voltage offset			150	µV[1]

Note: 1. Characterized on PCB, IC 100% tested.

2. Except in a 3-cell configuration, where 1.0 * NumCell < BAT+ < 1.8 * NumCell.

Ordering Information



*Requires configuration sheet (see Table 1)

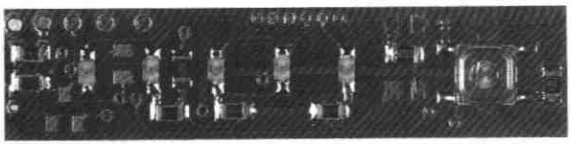
Notes

Preliminary **bq2111L**

Gas Gauge Module with LEDs

Features

- Complete bq2011 Gas Gauge solution for NiCd packs in high discharge rate applications
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring customized for 4- to 12-cell series applications (contact Benchmarq for greater than 12 cells)
- On-board regulator allows direct connection to the battery
- 5 surface-mounted LEDs to display state-of-charge information
- Nominal capacity pre-configured
- Compact size for battery pack integration



General Description

The bq2111L Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCD battery packs in high discharge rate applications such as power tools. Designed for battery pack integration, the bq2111L incorporates a bq2011 Gas Gauge IC, five surface-mounted LEDs, and the other discrete components necessary to accurately monitor the capacity of 4- to 12 series cells. The only external component required is a low-value sense resistor connected between GND and PACK-. Contacts are also provided on the bq2111L for direct connection to the battery stack and the serial communications port (DQ). The battery stack should be connected between BAT+ and GND. Please refer to the bq2011 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2111L based on the information requested in Table 1. The configuration defines the number of series cells and the nominal battery pack capacity. The bq2111L module uses the absolute LED display to indicate battery capacity. In this mode, the remaining capacity is represented as a percentage of the programmed full capacity.

The bq2111L can operate directly from 4 cells with no on-board regulation. In this configuration, Q3 and R13 are not placed on the board. For 4 series cell packs, LBAT+ should be connected to BATT. For greater than 4 series cell packs using the bq2011 regulator, Q3 and R13 are included and LBAT+ should be connected to BAT+. Please contact Benchmarq for gas gauging solutions for other battery chemistries or pack configurations greater than 12 series cells.

A module development kit is also available for the bq2111L. The bq2111LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2111L to display charge/discharge activity and to allow user interface to the bq2011 from any standard DOS PC.
3) Source code for the TSR.

Table 1. bq2111L Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

Number of series battery cells (4–12) _____

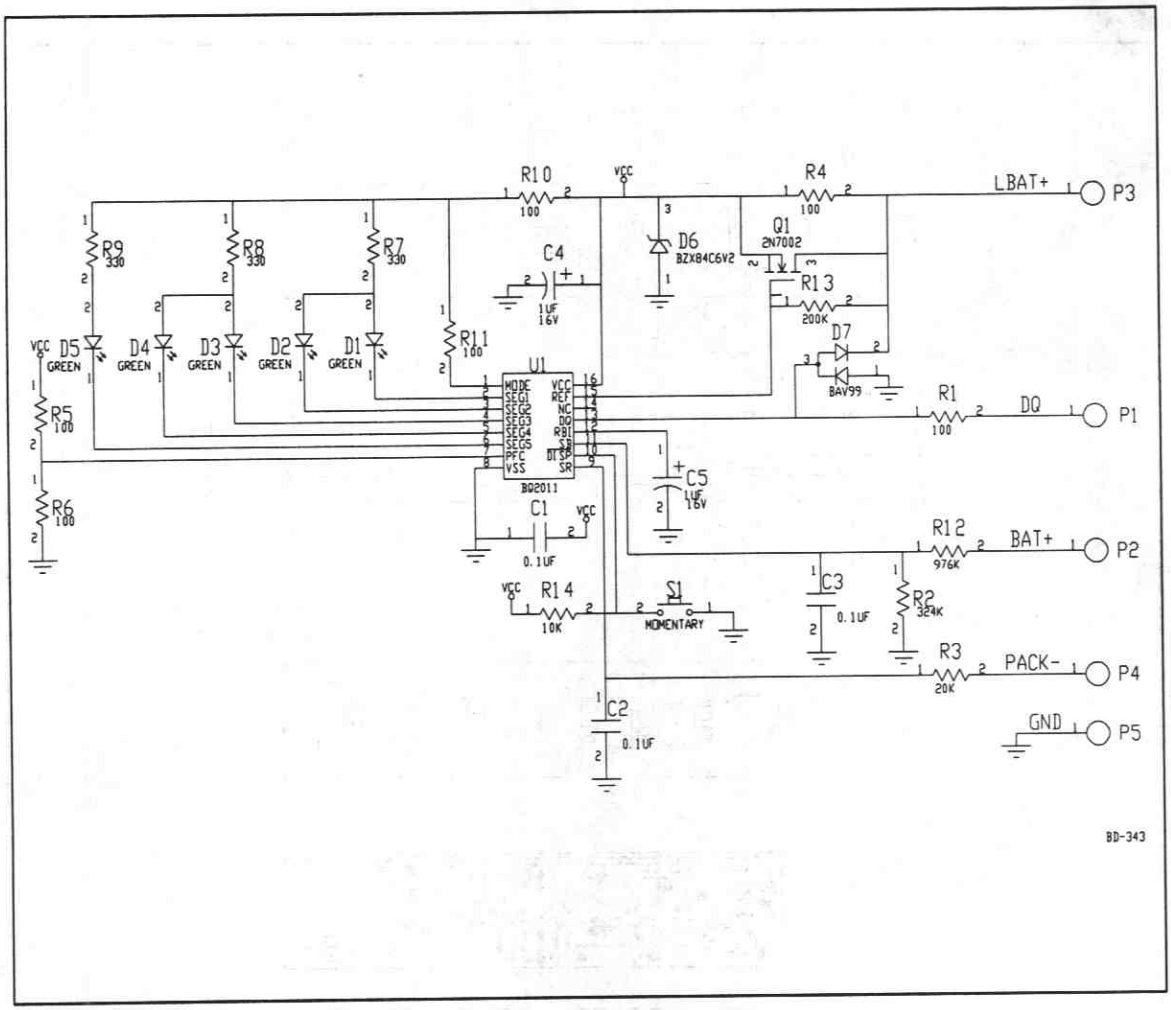
Sense resistor size in mΩ (0.005Ω standard)[1] _____

Battery pack capacity (mAh) _____

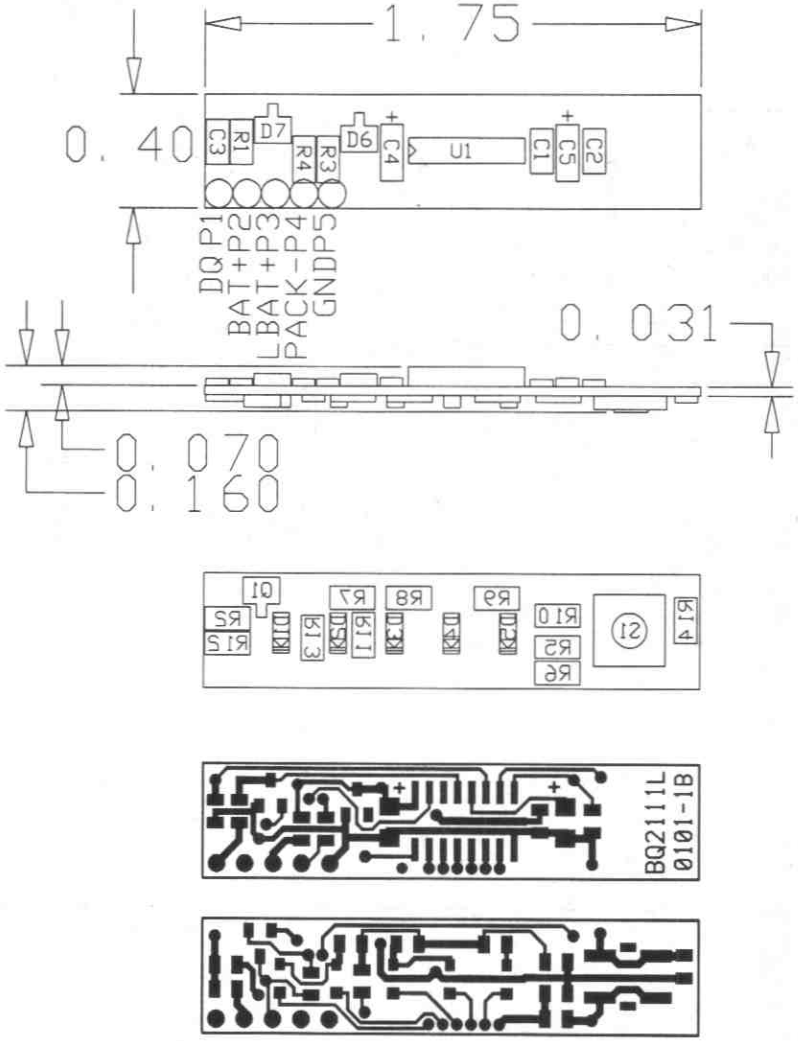
Note: 1. Sense resistor is not included with board.

Comments:

bq2111L Example Schematic



bq2111L Board



BD-344

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to Vss	-0.3	+7.0	V	
All other pins	Relative to Vss	-0.3	+7.0	V	
T_{OPR}	Operating temperature	0	+70	℃	Commercial
		-40	+85	℃	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (T_A = T_{OPR}; V_{CC} = 3.0 to 6.5V)

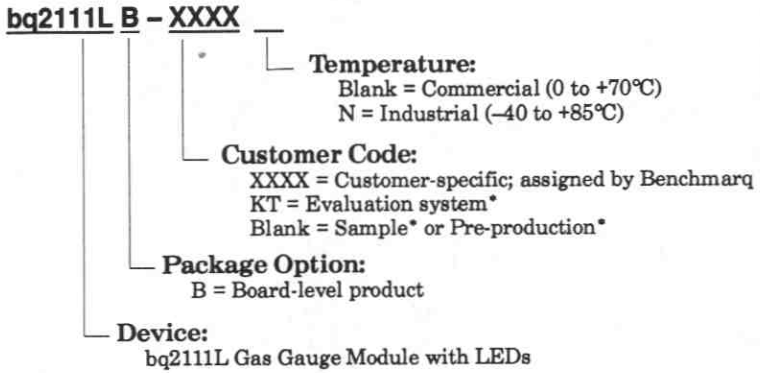
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	Final empty warning	0.87	0.90	0.93	V	SB, BAT+/NumCell
V_{SR1}	Discharge compensation threshold	20	50	75	mV	SR, V_{SR} + Vos
V_{SR2}	Discharge compensation threshold	70	100	125	mV	SR, V_{SR} + Vos
V_{SR3}	Discharge compensation threshold	120	150	175	mV	SR, V_{SR} + Vos
V_{SR4}	Discharge compensation threshold	220	253	275	mV	SR, V_{SR} + Vos
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + Vos
V_{SRQ}	Valid charge	-	-	-400	µV	V_{SR} + Vos
V_{SRD}	Valid discharge	500	-	-	µV	V_{SR} + Vos
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	SB, BAT+/NumCell
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB

DC Electrical Characteristics (T_A - T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
NumCell	Number of series cells in battery pack	4	-	12	-
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V
VSR	Voltage across the sense resistor	-0.3	-	2	V
V_{CC}	Supply voltage, 0.87 * NumCell < LBAT+ < 1.8 * NumCell	3.0	4.25	6.5	V
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	120	250	µA
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]
I_{OL}	Open-drain sink current DQ	-	-	5.0	mA[1]
V_{OL}	Open-drain output low, I_{OL} < 5mA, DQ	-	-	0.5	V[1]
V_{IHDQ}	DQ input high	2.5	-	-	V[1]
V_{ILDQ}	DQ input low	-	-	0.8	V[1]
V_{OS}	Voltage offset			150	µV[1]

Note: 1. Characterized on PCB, IC 100% tested.

Ordering Information



*Requires configuration sheet (see Table 1)

Notes

bq2112

Gas Gauge Module

Features

- Complete bq2012 Gas Gauge solution for NiCd or NiMH battery packs
- Charge control output
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring customized for 3- to 12-cell series applications (contact Benchmarq for greater than 12 cells)
- On-board regulator allows direct connection to the battery
- Contacts for 6 LED outputs for state-of-charge information display
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration

General Description

The bq2112 Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCD and NiMH battery packs. Designed for battery pack integration, the bq2112 incorporates a bq2012 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor the capacity of 3 to 12 series cells. Contacts are provided on the bq2112 for direct connection to the battery stack (BAT+, BAT-), six LEDs, the serial communications port (DQ), the empty indicator (EMPTY), the display control input ($\overline{\text{DISP}}$), and the charge control output ($\overline{\text{CHG}}$). Please refer to the bq2012 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2112 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode. Please contact Benchmarq for gas gauging solutions for other battery chemistries or pack configurations greater than 12 series cells.

The onboard sense resistor accurately measures the charge and discharge activity of the battery pack. The resistor value and type should be specified on the configuration sheet. To minimize module height, a surface mount (SMD) sense resistor can be selected. Refer to page 4 for the bq2112 physical dimensions.

A module development kit is also available for the bq2112. The bq2112B-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2112 to display charge/discharge activity and to allow user interface to the bq2012 from any standard DOS PC.
3) Source code for the TSR.

Table 1. bq2112 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

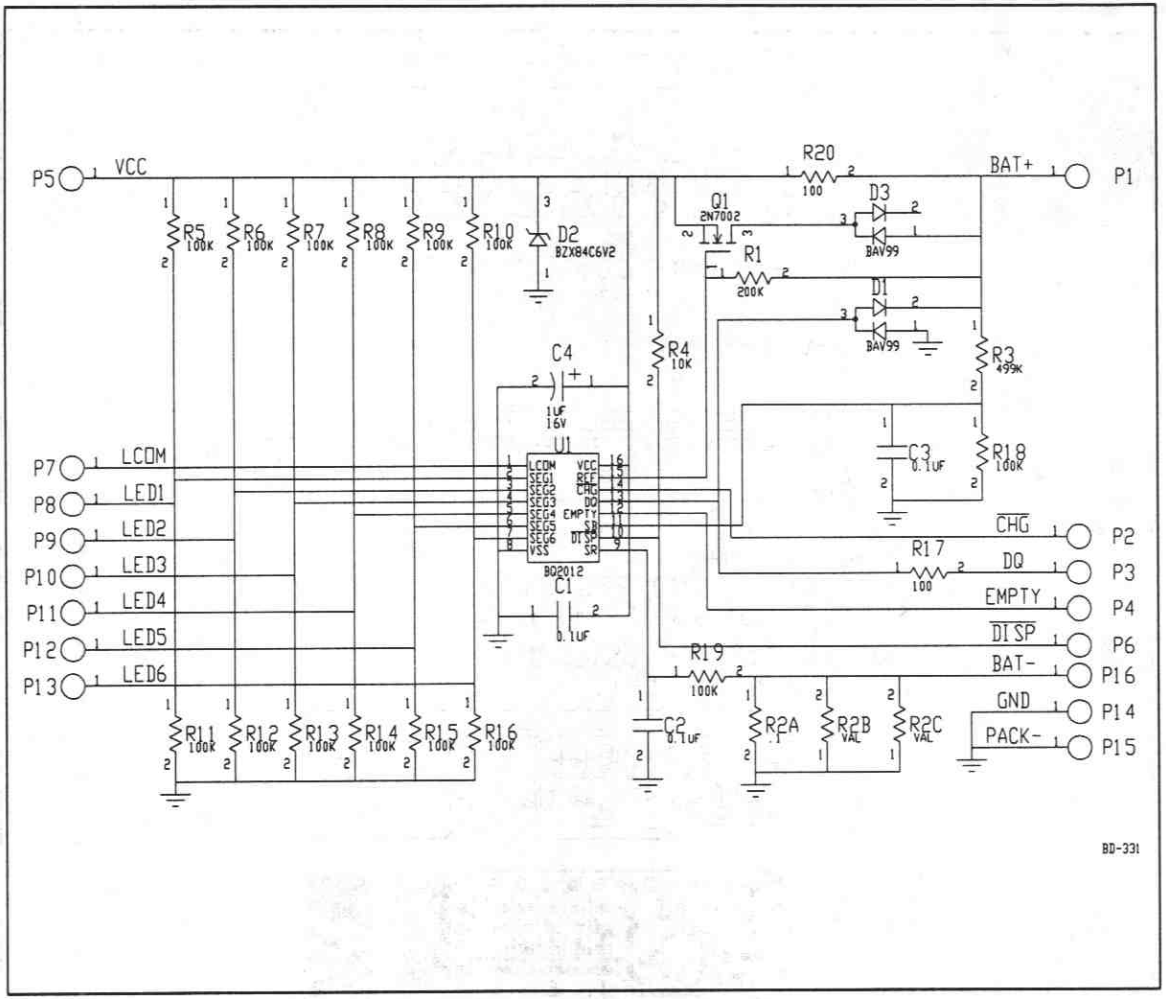
_____

Sales Contact: _____ Phone: _____

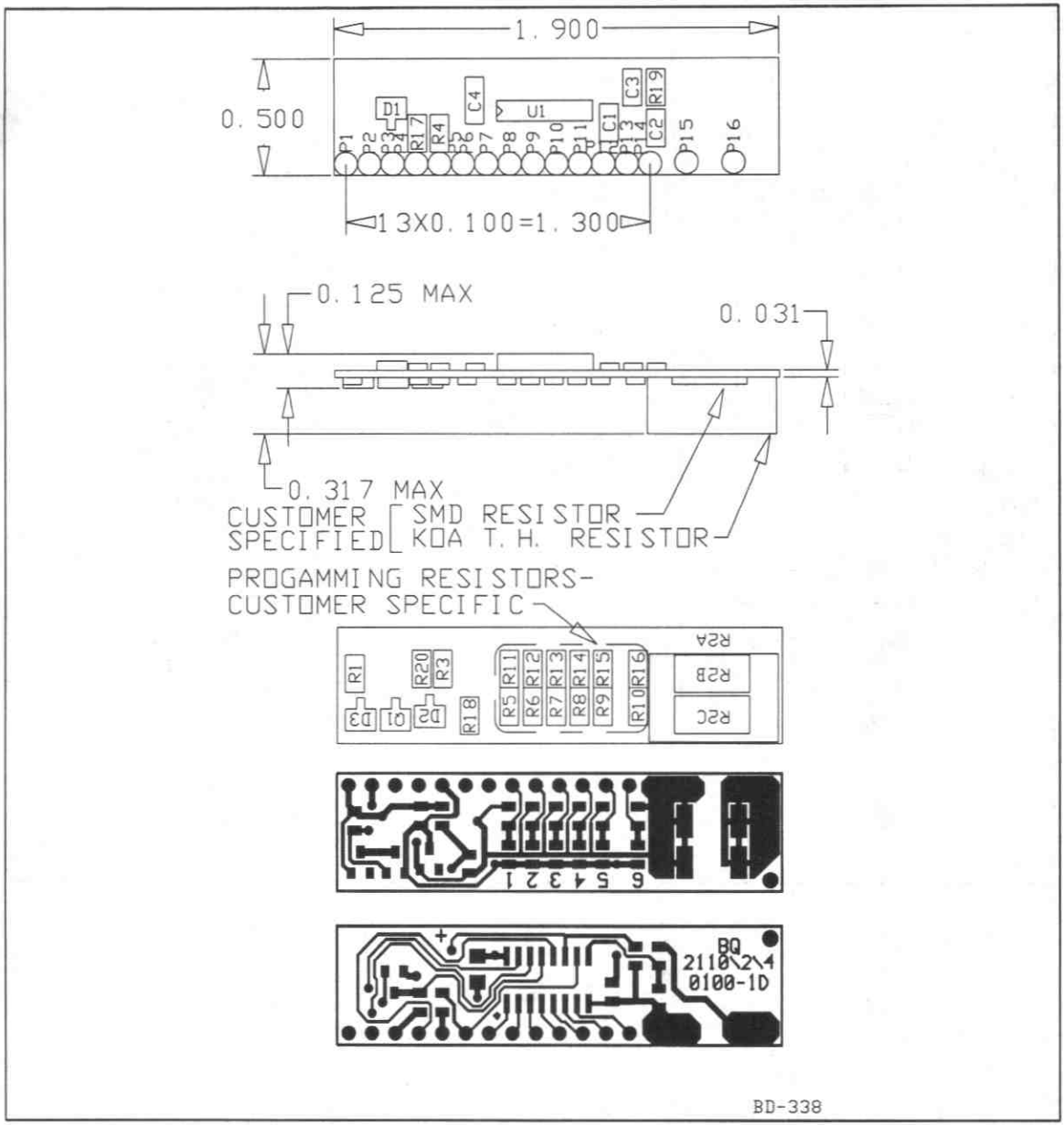
Number of series battery cells (3–12)	_____
Sense resistor size in mΩ (0.1Ω standard)	_____
Sense resistor type: KOA(2W), SMD(1W), 2xSMD(1W)	_____
Battery pack capacity (mAh)	_____
Battery type (NiCd or NiMH)	_____
Display mode (absolute or relative)	_____

Comments:

bq2112 Example Schematic



bq2112 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
P_{SR}	Continuous sense resistor power dissipation	-	2	W	KOA sense resistor
		-	2	W	2 SMT sense resistors in parallel
		-	1	W	SMT sense resistor
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (T_A = T_{OPR}; V_{CC} = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB, BAT+/NumCell
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB, BAT+/NumCell
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, V_{SR} + V_{OS}
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	375	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-300	µV	V_{SR} + V_{OS} (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB, BAT+/NumCell
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Note: Default value; value set in DMF register.

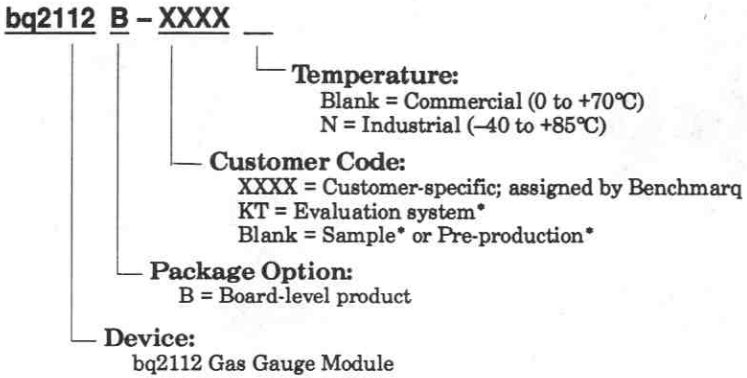
DC Electrical Characteristics (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
NumCell	Number of series cells in battery pack	3	-	12	-
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V
V_{CC}	Supply voltage, 0.93 * NumCell < BAT+ < 1.8 * NumCell[2]	3.0	4.25	6.5	V
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]
R_{DISP}	Pull-up	-	10K	-	Ω
V_{OLSL}	SEGx output low, V_{CC} = 3.0, I_{OLS} < 1.75mA	-	0.1	-	V[1]
V_{OLSH}	SEGx output low, V_{CC} = 6.5, I_{OLS} < 1.75mA	-	0.4	-	V[1]
V_{OHLCL}	LCOM output high, V_{CC} = 3.0, I_{OHLCOM} - -5.25mA	V_{CC} - 0.3	-	-	V[1]
V_{OHLCH}	LCOM output high, V_{CC} = 6.5, I_{OHLCOM} - -33.0mA	V_{CC} - 0.6	-	-	V[1]
I_{OHLCOM}	LCOM source current	-33.0	-	-	mA[1]
I_{OLS}	SEGx sink current	-	-	11.0	mA[1]
I_{OL}	Open-drain sink current DQ, EMPTY, $\overline{CHG}$	-	-	5.0	mA[1]
V_{OL}	Open-drain output low, I_{OL} < 5mA, DQ, EMPTY	-	-	0.5	V[1]
V_{IHDQ}	DQ input high	2.5	-	-	V[1]
V_{ILDQ}	DQ input low	-	-	0.8	V[1]
V_{OS}	Voltage offset			150	µV[1]

Notes: 1. Characterized on PCB, IC 100% tested.

2. Except in a 3-cell configuration, where 1.0 * NumCell < BAT+ < 1.8 * NumCell.

Ordering Information



*Requires configuration sheet (see Table 1)

Notes

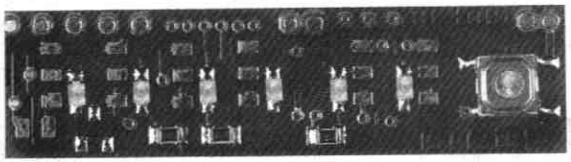
BENCHMARQ

bq2112L

Gas Gauge Module With LEDs

Features

- Complete bq2012 Gas Gauge solution for NiCd or NiMH battery packs
- Charge control output
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring customized for 3- to 12-cell series applications (contact Benchmarq for greater than 12 cells)
- On-board regulator allows direct connection to the battery
- 6 surface-mounted LEDs to display state-of-charge information
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration



General Description

The bq2112L Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCD and NiMH battery packs. Designed for battery pack integration, the bq2112L incorporates a bq2012 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 3 to 12 series cells. Contacts are provided on the bq2112L for direct connection to the battery stack (BAT+, BAT-), the serial communications port (DQ), the empty indicator (EMPTY), and the charge control output (CHG). Please refer to the bq2012 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2112L based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode. Please contact Benchmarq for gas gauging solutions for other battery chemistries or pack configurations greater than 12 series cells.

The onboard sense resistor accurately measures the charge and discharge activity of the battery pack. The resistor value and type should be specified on the configuration sheet. To minimize module height, a surface mount (SMD) sense resistor can be selected. Refer to page 4 for the bq2112L physical dimensions.

A module development kit is also available for the bq2112L. The bq2112LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2112L to display charge/discharge activity and to allow user interface to the bq2012 from any standard DOS PC.
3) Source code for the TSR.

Table 1. bq2112L Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

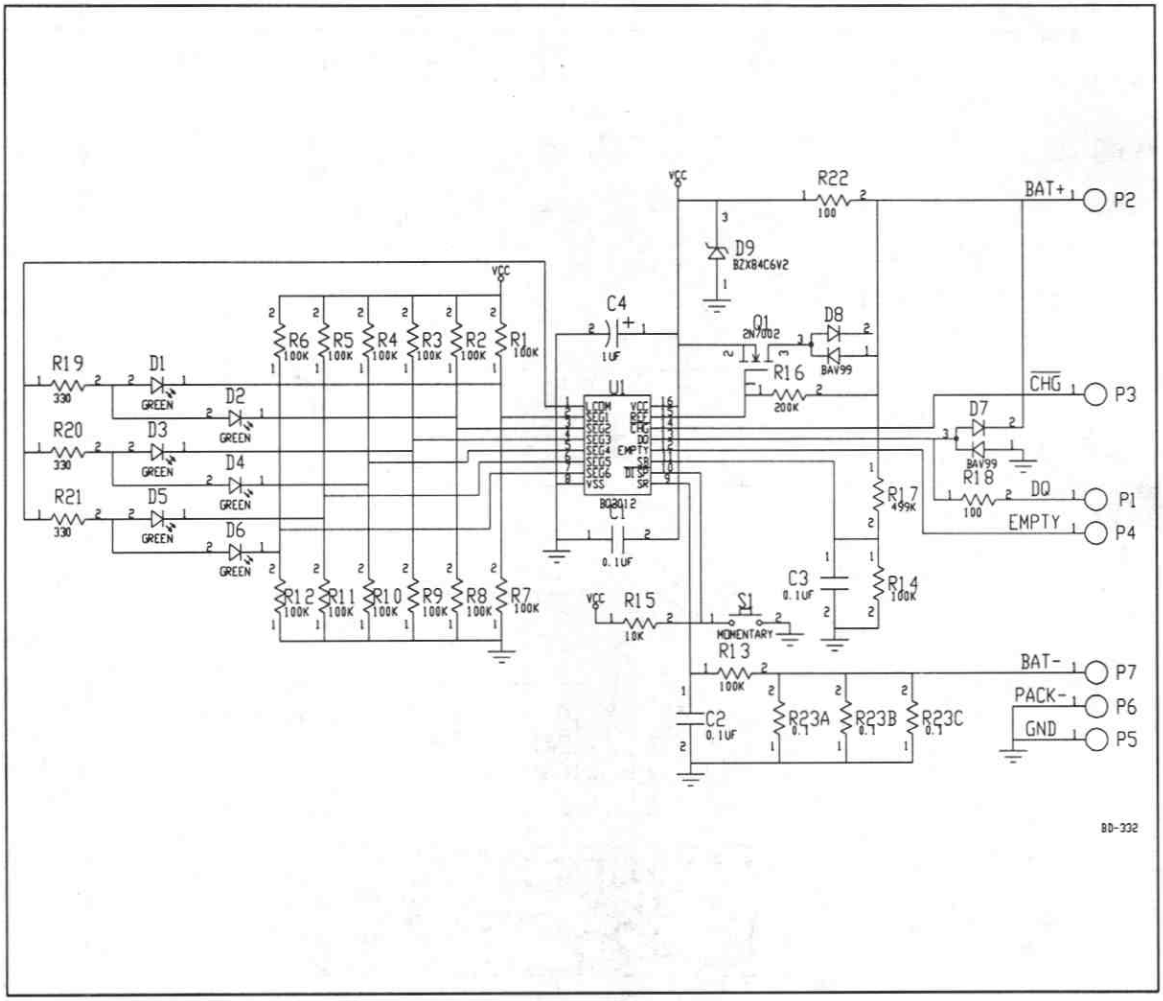
_____

Sales Contact: _____ Phone: _____

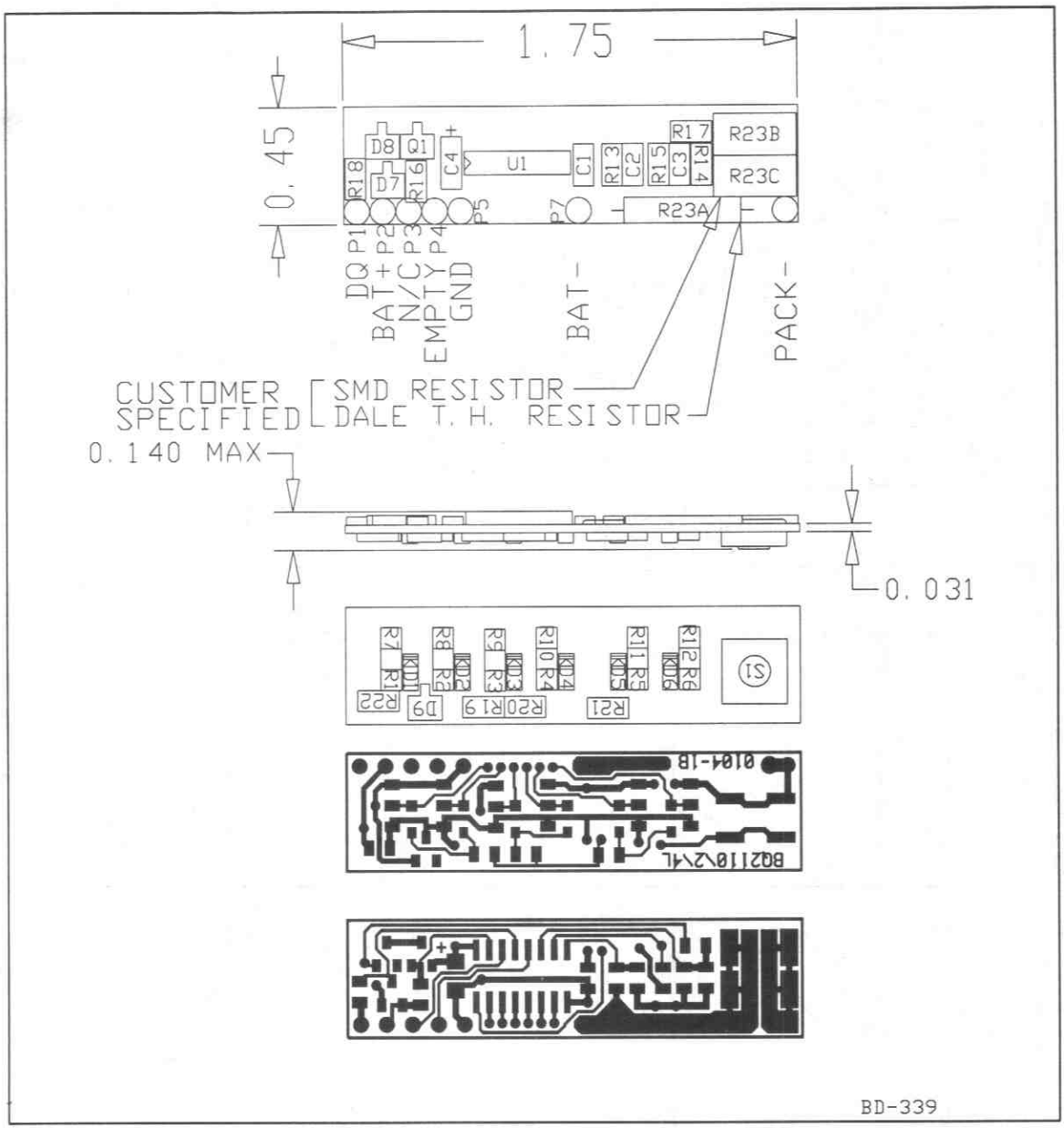
Number of series battery cells (3–12)	_____
Sense resistor size in mΩ (0.1Ω standard)	_____
Sense resistor type: DALE(3W), SMD(1W), 2xSMD(1W)	_____
Battery pack capacity (mAh)	_____
Battery type (NiCd or NiMH)	_____
Display mode (absolute or relative)	_____

Comments:

bq2112L Example Schematic



bq2112L Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
P_{SR}	Continuous sense resistor power dissipation	-	3	W	DALE sense resistor
		-	2	W	2 SMT sense resistors in parallel
		-	1	W	SMT sense resistor
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V_{CC} = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB, BAT+/NumCell
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB, BAT+/NumCell
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, V_{SR} + V_{OS}
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	375	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-300	µV	V_{SR} + V_{OS} (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB, BAT+/NumCell
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Note: Default value; value set in DMF register.

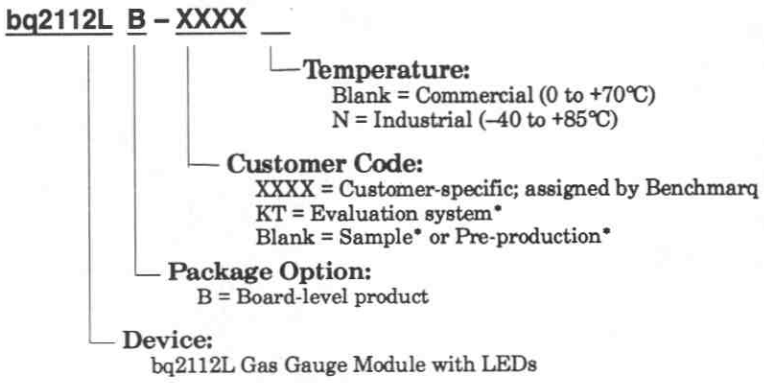
DC Electrical Characteristics (T_A - T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
NumCell	Number of series cells in battery pack	3	-	12	-
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V
V_{CC}	Supply voltage, 0.93 * NumCell < BAT+ < 1.8 * NumCell[2]	3.0	4.25	6.5	V
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]
I_{OL}	Open-drain sink current DQ, EMPTY, $\overline{CHG}$	-	-	5.0	mA[1]
V_{OL}	Open-drain output low, I_{OL} < 5mA, DQ, EMPTY	-	-	0.5	V[1]
V_{IHDQ}	DQ input high	2.5	-	-	V[1]
V_{ILDQ}	DQ input low	-	-	0.8	V[1]
V_{OS}	Voltage offset			150	µV[1]

Notes: 1. Characterized on PCB, IC 100% tested.

2. Except in a 3-cell configuration, where 1.0 * NumCell < BAT+ < 1.8 * NumCell.

Ordering Information



*Requires configuration sheet (see Table 1)

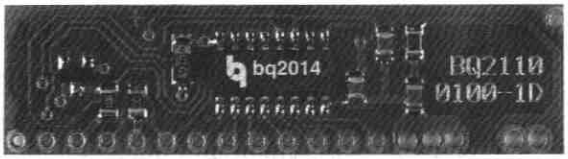
Notes

Preliminary bq2114

Gas Gauge Module

Features

- Complete bq2014 Gas Gauge solution for NiCd or NiMH battery packs
- Charge control output and charge complete input allow communication to external charge controller
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring customized for 3- to 12-cell series applications (contact Benchmarq for greater than 12 cells)
- On-board regulator allows direct connection to the battery
- Contacts for 5 LED outputs for state-of-charge information display
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration



General Description

The bq2114 Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCD and NiMH battery packs. Designed for battery pack integration, the bq2114 incorporates a bq2014 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor the capacity of 3 to 12 series cells. Contacts are provided on the bq2114 for the following:

- Direct connection to the battery stack (BAT+, BAT-)
- Five LEDs
- The serial communications port (DQ)
- The empty indicator (EMPTY)
- The display control input ($\overline{\text{DISP}}$)
- The battery charge complete (DONE) inputs
- The battery charge control output (CHG).

Please refer to the bq2014 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2114 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode. Please contact Benchmarq for gas gauging solutions for other battery chemistries or pack configurations greater than 12- series cells.

The onboard sense resistor accurately measures the charge and discharge activity of the battery pack. The resistor value and type should be specified on the configuration sheet. To minimize module height, a surface mount (SMD) sense resistor can be selected. Refer to page 4 for the bq2114 physical dimensions.

A module development kit is also available for the bq2114. The bq2114B-KT includes one configured module and the following:

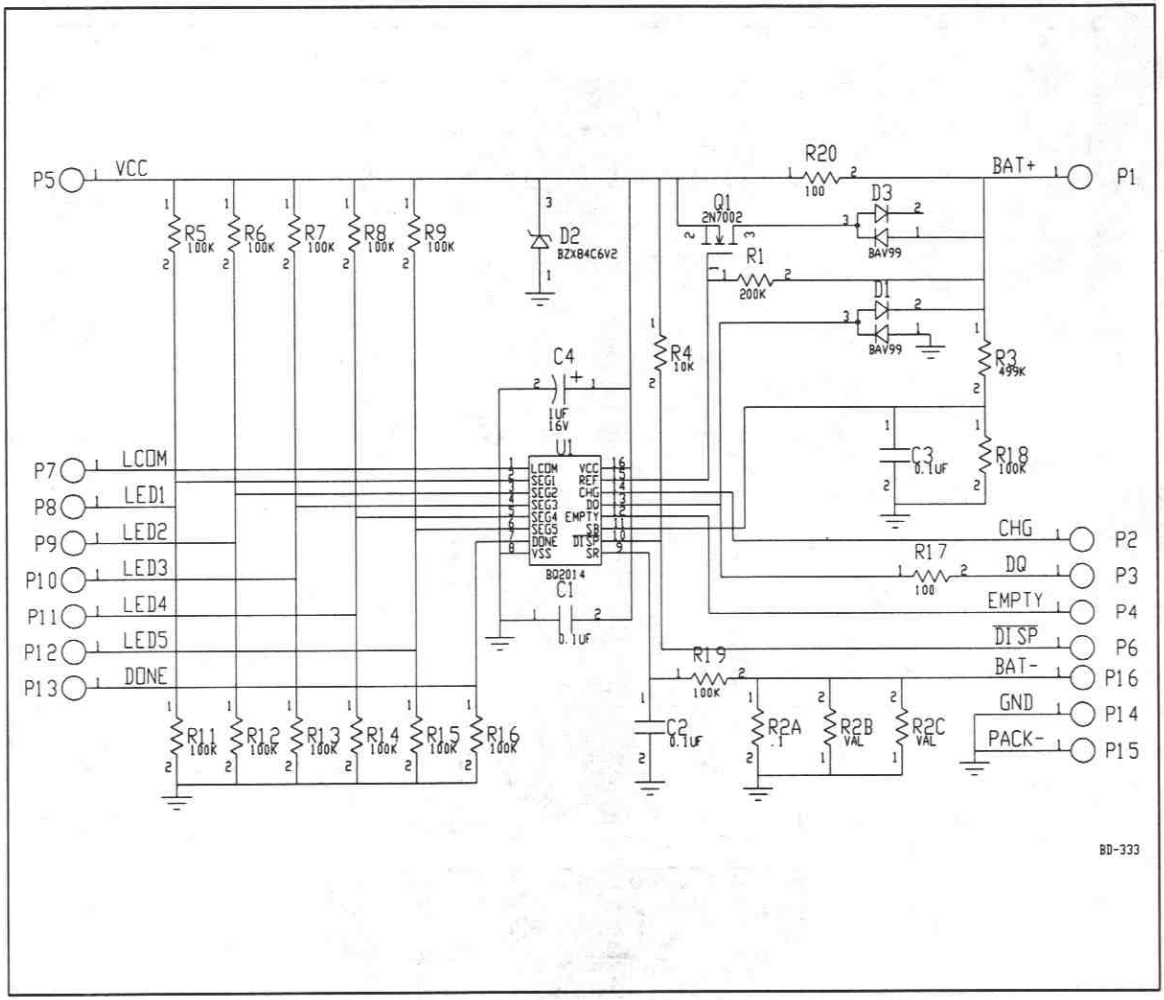
1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2114 to display charge/discharge activity and to allow user interface to the bq2014 from any standard DOS PC.
3) Source code for the TSR.

Table 1. bq2114 Module Configuration

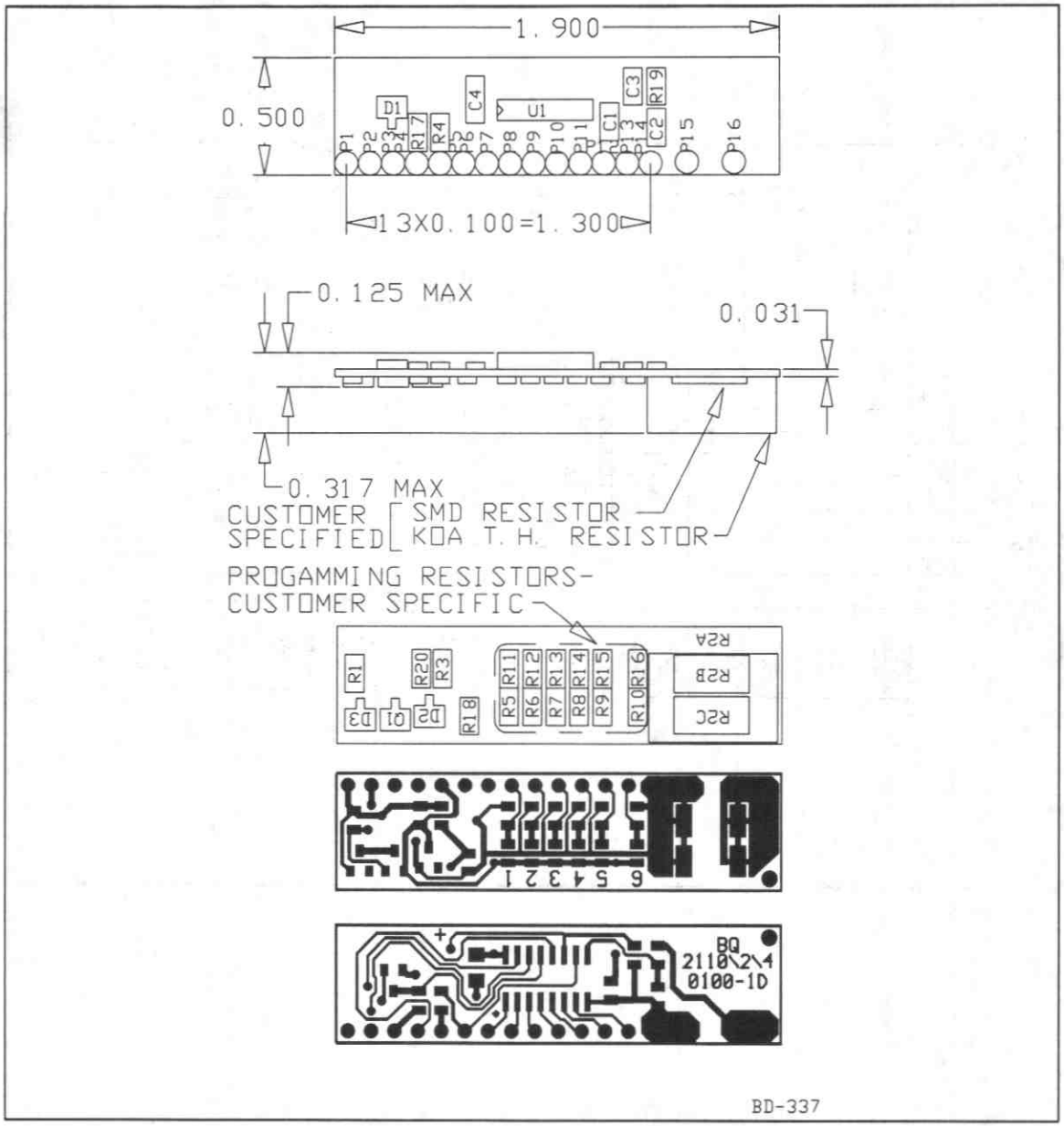
Customer Name:	
Contact:	Phone:
Address:	
Sales Contact:	Phone:
Number of series battery cells (3–12)	
Sense resistor size in mΩ (0.1Ω standard)	
Sense resistor type: KOA(2W), SMD(1W), 2xSMD(1W)	
Battery pack capacity (mAh)	
Battery type (NiCd or NiMH)	
Display mode (absolute or relative)	

Comments:

bq2114 Example Schematic



bq2114 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
P_{SR}	Continuous sense resistor power dissipation	-	2	W	KOA sense resistor
		-	2	W	2 SMT sense resistors in parallel
		-	1	W	SMT sense resistor
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V_{CC} = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB, BAT+/NumCell
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB, BAT+/NumCell
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, V_{SR} + V_{OS}
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	375	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-300	µV	V_{SR} + V_{OS} (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB, BAT+/NumCell
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Note: Default value; value set in DMF register.

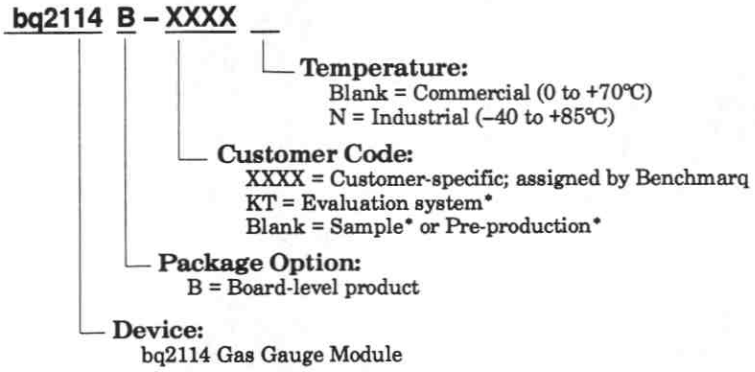
DC Electrical Characteristics (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
NumCell	Number of series cells in battery pack	3	-	12	-
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V
V_{CC}	Supply voltage, 0.93 * NumCell < BAT+ < 1.8 * NumCell [2]	3.0	4.25	6.5	V
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]
R_{DISP}	Pull-up	-	10K	-	Ω
V_{OLSL}	SEGx output low, V_{CC} = 3.0, I_{OLS} < 1.75mA	-	0.1	-	V[1]
V_{OLSH}	SEGx output low, V_{CC} = 6.5, I_{OLS} < 1.75mA	-	0.4	-	V[1]
V_{OHLCL}	LCOM output high, V_{CC} = 3.0, I_{OHLCOM} - - 5.25mA	V_{CC} - 0.3	-	-	V[1]
V_{OHLCH}	LCOM output high, V_{CC} = 6.5, I_{OHLCOM} - - 33.0mA	V_{CC} - 0.6	-	-	V[1]
I_{OHLCOM}	LCOM source current	-33.0	-	-	mA[1]
I_{OLS}	SEGx sink current	-	-	11.0	mA[1]
I_{OL}	Open-drain sink current DQ, EMPTY, CHG	-	-	5.0	mA[1]
V_{OL}	Open-drain output low, I_{OL} < 5mA, DQ, EMPTY	-	-	0.5	V[1]
V_{IHDQ}	DQ input high	2.5	-	-	V[1]
V_{ILDQ}	DQ input low	-	-	0.8	V[1]
V_{OS}	Voltage offset			150	µV[1]

Note: 1. Characterized on PCB, IC 100% tested.

2. Except in a 3-cell configuration, where 1.0 * NumCell < BAT+ < 1.8 * NumCell.

Ordering Information



*Requires configuration sheet (see Table 1)

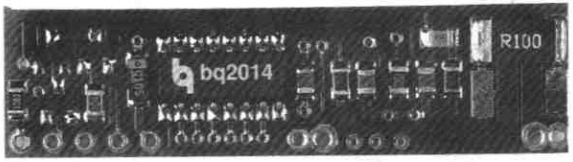
Notes

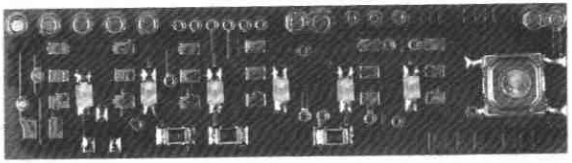
Preliminary bq2114L

Gas Gauge Module with LEDs

Features

- Complete bq2014 Gas Gauge solution for NiCd or NiMH battery packs
- Charge control output and charge complete input allow communication to external charge controller
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring customized for 3- to 12-cell series applications (contact Benchmarq for greater than 12 cells)
- On-board regulator allows direct connection to the battery
- 5 surface-mounted LEDs for state-of-charge information
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration





General Description

The bq2114L Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCD and NiMH battery packs. Designed for battery pack integration, the bq2114L incorporates a bq2014 Gas Gauge IC, a current sense resistor, five surface-mounted LEDs, and all other components necessary to accurately monitor and display the capacity of 3 to 12 series cells. Contacts are provided on the bq2114L for direct connection to the battery stack (BAT+, BAT-), the serial communications port (DQ), the empty indicator (EMPTY), the battery charge complete input (DONE), and the battery charge control output (CHG). Please refer to the bq2014 data sheet for the specifics on the operation of the Gas Gauge.

Benchmarq configures the bq2114L based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode. Please contact Benchmarq for gas gauging solutions for other battery chemistries or pack configurations greater than 12 series cells.

The onboard sense resistor accurately measures the charge and discharge activity of the battery pack. The resistor value and type should be specified on the configuration sheet. To minimize module height, a surface mount (SMD) sense resistor can be selected. Refer to page 4 for the bq2114L physical dimensions.

A module development kit is also available for the bq2114L. The bq2114LB-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2114L to display charge/discharge activity and to allow user interface to the bq2014 from any standard DOS PC.
3) Source code for the TSR.

Table 1. bq2114L Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

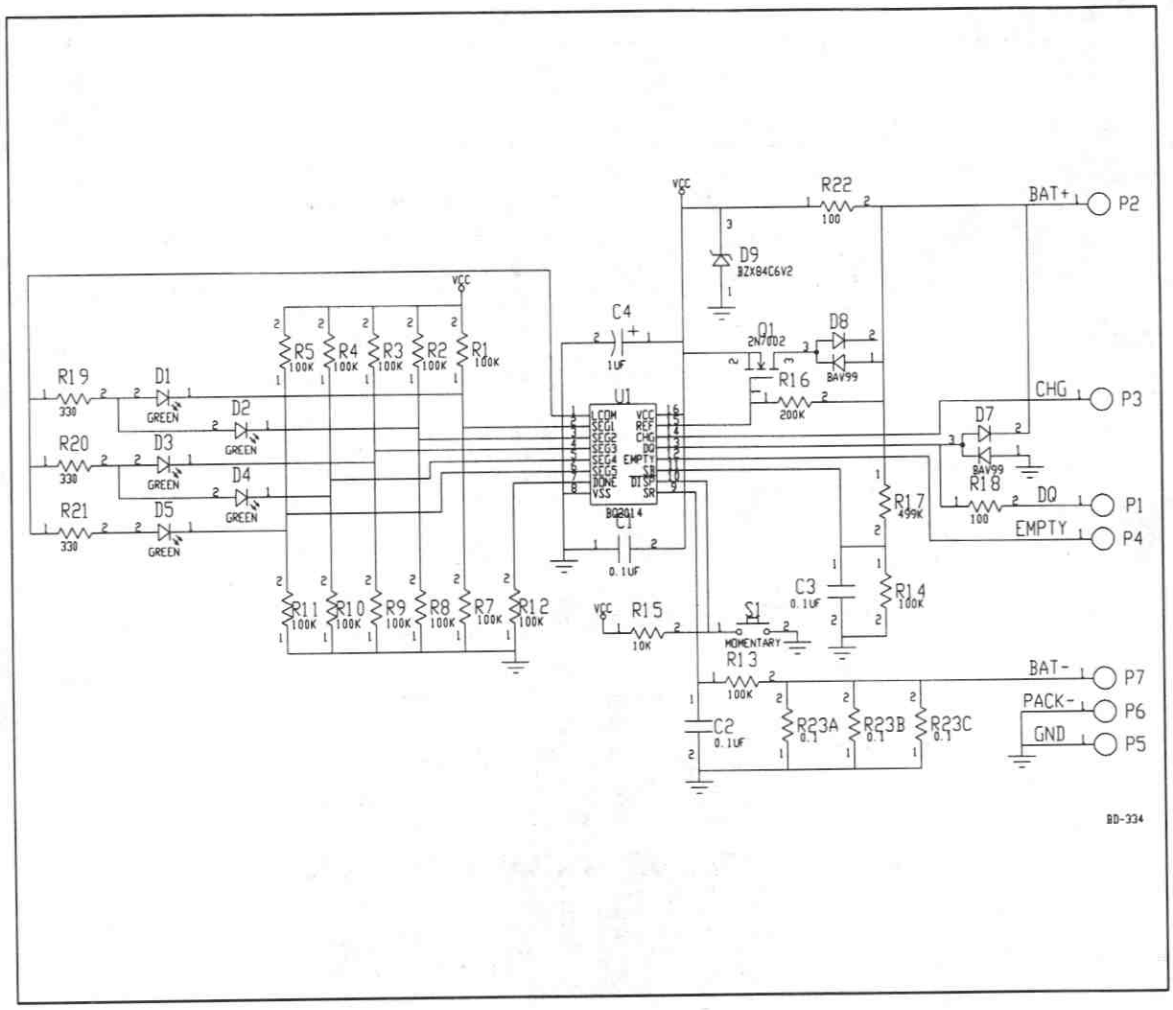
_____

Sales Contact: _____ Phone: _____

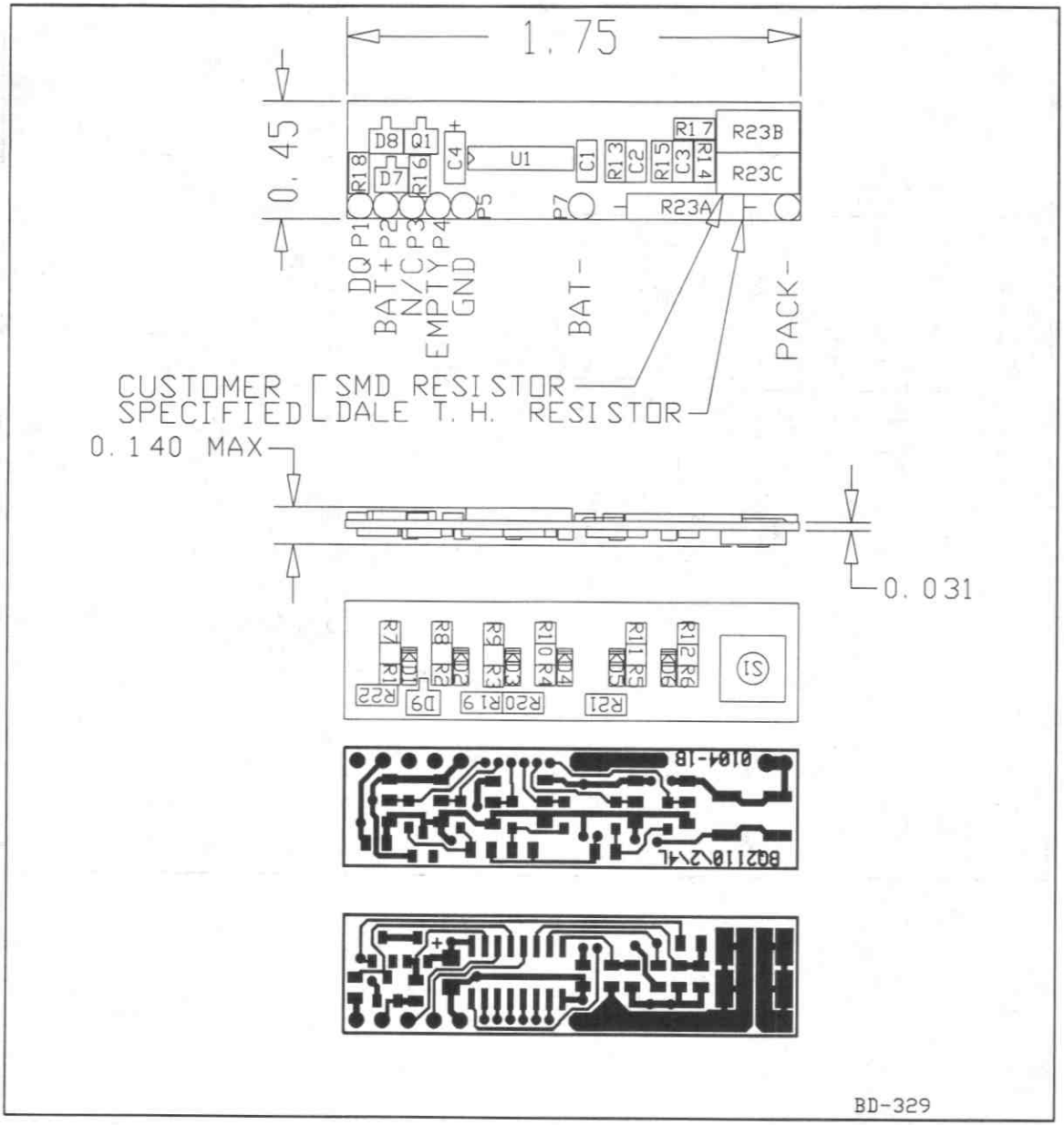
Number of series battery cells (3–12)	_____
Sense resistor size in mΩ (0.1Ω standard)	_____
Sense resistor type: DALE(3W), SMD(1W), 2xSMD(1W)	_____
Battery pack capacity (mAh)	_____
Battery type (NiCd or NiMH)	_____

Comments:

bq2114L Example Schematic



bq2114L Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to Vss	-0.3	+7.0	V	
All other pins	Relative to Vss	-0.3	+7.0	V	
P_{SR}	Continuous sense resistor power dissipation	-	3	W	DALE sense resistor
		-	2	W	2 SMT sense resistors in parallel
		-	1	W	SMT sense resistor
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V_{CC} = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB, BAT+/NumCell
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB, BAT+/NumCell
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, V_{SR} + V_{OS}
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	375	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-300	µV	V_{SR} + V_{OS} (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB, BAT+/NumCell
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Note: Default value; value set in DMF register.

DC Electrical Characteristics (T_A - T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
NumCell	Number of series cells in battery pack	3.0	-	12.0	-
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V
V_{CC}	Supply voltage, 0.93 * NumCell < BAT+ < 1.8 * NumCell[2]	3.0	4.25	6.5	V
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]
I_{OL}	Open-drain sink current DQ, EMPTY, CHG	-	-	5.0	mA[1]
V_{OL}	Open-drain output low, I_{OL} < 5mA, DQ, EMPTY	-	-	0.5	V[1]
V_{IHDQ}	DQ input high	2.5	-	-	V[1]
V_{ILDQ}	DQ input low	-	-	0.8	V[1]
V_{OS}	Voltage offset			150	µV[1]

Notes: 1. Characterized on PCB, IC 100% tested.

2. Except in a 3-cell configuration, where 1.0 * NumCell < BAT+ < 1.8 * NumCell.

Ordering Information

bq2114L B – XXXX __

Temperature:
Blank = Commercial (0 to +70°C)
N = Industrial (–40 to +85°C)

Customer Code:
XXXX = Customer-specific; assigned by Benchmarq
KT = Evaluation system*
Blank = Sample* or Pre-production*

Package Option:
B = Board-level product

Device:
bq2114L Gas Gauge Module with LEDs

*Requires configuration sheet (see Table 1)

Notes

Preliminary **bq2164**

Gas Gauge Module With Fast Charge Control

Features

- Complete bq2004/bq2014 battery management solution for NiCd or NiMH pack
- Accurate battery state-of-charge monitoring
- Reliable fast charge termination
- Automatic full capacity calibration
- Battery information available over a single-wire bi-directional serial port
- Nominal capacity, cell chemistry, and charge control parameters pre-configured
- Compact size for battery pack integration

General Description

The bq2164 Gas Gauge Module provides a complete and compact battery management solution for NiCd and NiMH battery packs. Designed for battery pack integration, the bq2164 combines the bq2014 Gas Gauge IC with the bq2004 Fast Charge IC on a small printed circuit board. The board includes all the necessary components to accurately monitor the capacity and reliably terminate fast charge of 5 to 12 series cells.

The gas gauge IC uses the onboard sense resistor to track charge and discharge activity of the battery pack. The fast charge IC gates a current-limited or constant-current charging supply connected to PACK+. Charging termination is based on $\Delta T/\Delta t$ or $-\Delta V/PVD$, maximum temperature, time, and voltage. The bq2004 signals charge completion to the bq2014 to indicate full capacity. The charge complete signal to the gas gauge eliminates the need to fully cycle the battery pack to initially calibrate full pack capacity.

Contacts are provided on the bq2164 for direct connection to the battery stack (BAT+, BAT-), the gas gauge's communications port (DQ), and the thermistor (THERM+, THERM). The thermistor is required for temperature fast charge termination. Please refer to the bq2004 and bq2014 data sheets for the specifics on the operation of the gas gauge and the fast charge ICs.

Benchmarq configures the bq2164 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the fast charge control parameters. The control parameters depend on the charge rate, cell chemistry and termination technique specified in the configuration table. They consist of the fast charge hold-off and safety timers, the use of a top-off period, and the pulse trickle rate as shown on page 7 of the bq2004 data sheet. The bq2164 is optimized for temperature termination with the thermistor provided. Please contact Benchmarq for gas gauging and fast charge solutions for other battery chemistries or pack configurations greater than 12 series cells.

The sense resistor value and type should also be specified on the configuration sheet. To minimize module height, a surface mount (SMD) sense resistor can be selected. Refer to Page 4 for the bq2164 physical dimensions.

A module development kit is also available for the bq2164. The bq2164B-KT includes one configured module and the following:

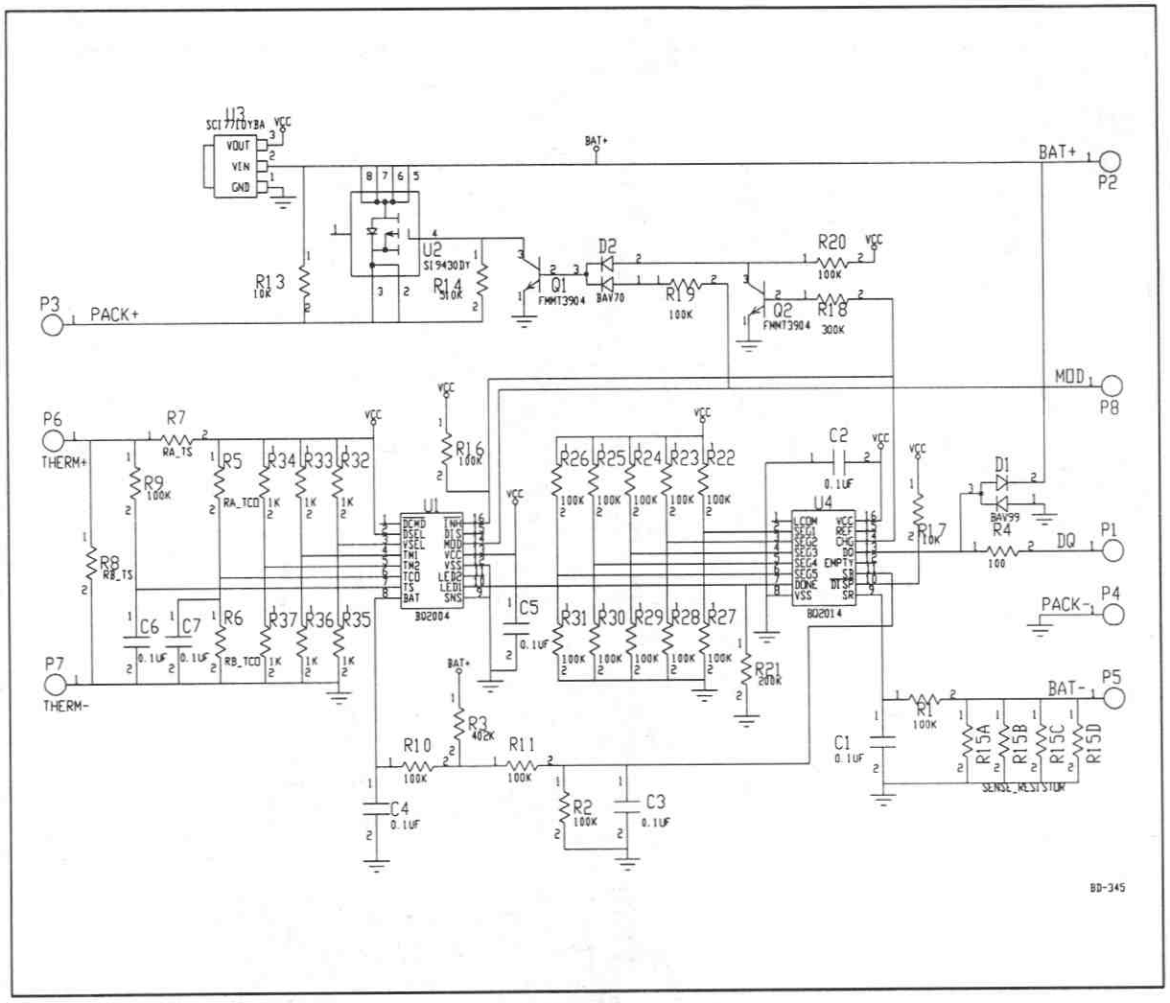
1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2164 to display charge/discharge activity and to allow user interface to the bq2014 from any standard DOS PC.
3) Source code for the TSR.

Table 1. bq2164 Module Configuration

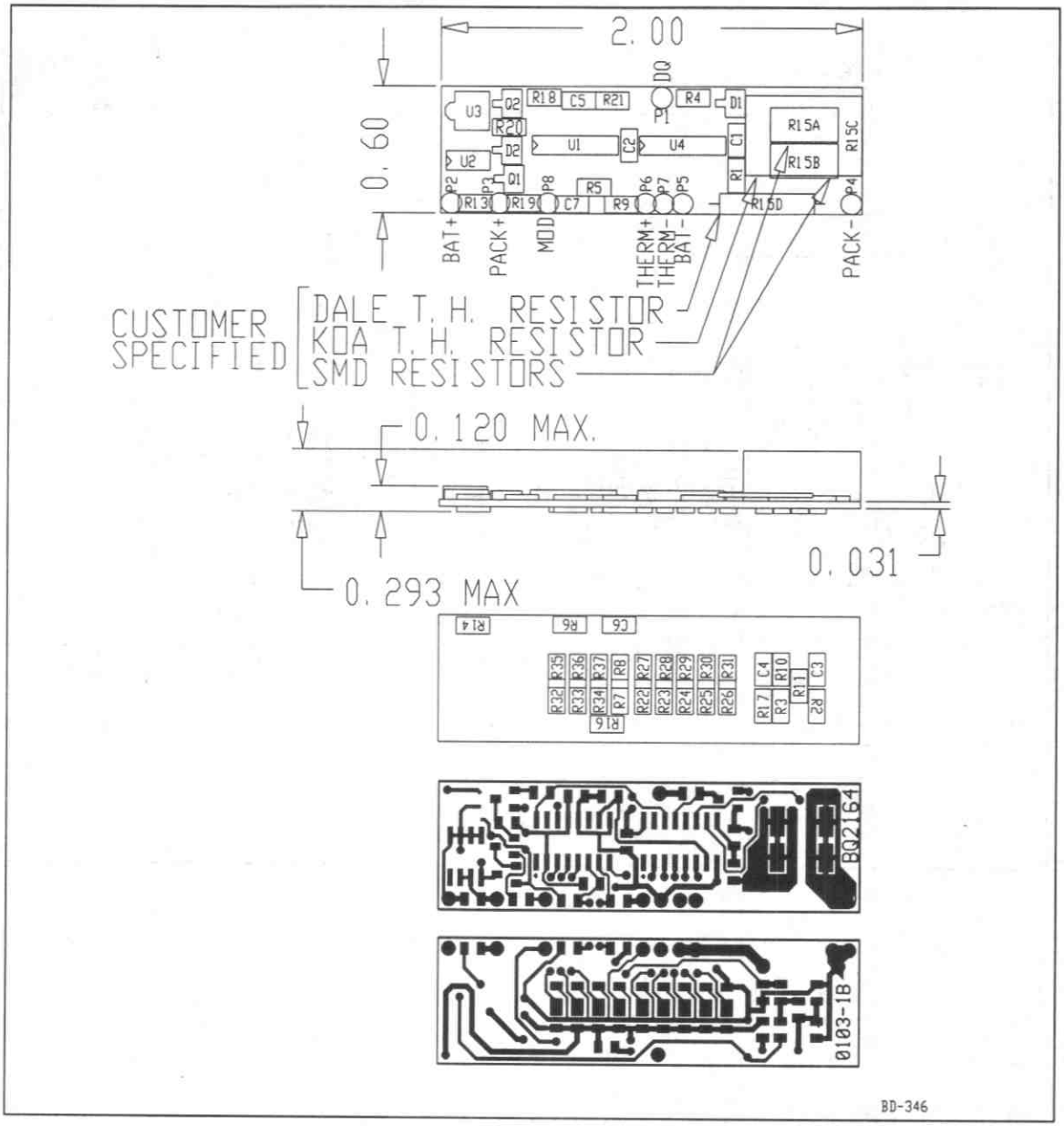
Customer Name:	
Contact:	Phone:
Address:	
Sales Contact:	Phone:
Number of series battery cells (5–12)	
Sense resistor size in mΩ (0.1Ω standard)	
Sense resistor type: DALE (3W), KOA(2W), SMD(1W), 2xSMD(1W)	
Battery pack capacity (mAh)	
Battery type (NiCd or NiMH)	
Fast charge current (A)	
Top-off (Y/N)	
Charge voltage (V)	
Temperature termination (enabled/disabled)	
PVD or –ΔV termination	

Comments:

bq2164 Example Schematic



bq2164 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
P_{SR}	Continuous sense resistor power dissipation	-	3	W	DALE sense resistor
		-	2	W	KOA sense resistor
		-	2	W	2 SMT sense resistors in parallel
		-	1	W	SMT sense resistor
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage and Temperature Thresholds (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB, BAT+/NumCell
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB, BAT+/NumCell
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, V_{SR} + V_{OS}
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	375	-	-	µV	V_{SR} + V_{OS} [1]
V_{SRD}	Valid discharge	-	-	-300	µV	V_{SR} + V_{OS} [1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB, BAT+/NumCell
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high
T_{LTF}	Low temperature charging fault	-	10	-	°C	Low temperature charge inhibit/terminate [2]
T_{HTF}	High temperature charging fault	-	45	-	°C	High temperature charge inhibit
V_{EDVC}	Minimum charging cell voltage	-	1	-	V	Minimum cell voltage to initiate charge
V_{MCVC}	Maximum charging cell voltage	-	2	-	V	Maximum cell voltage to initiate or continue charge
$R_{\Delta T/\Delta t}$	$\Delta T/\Delta t$ charge termination rate	-	1	-	°C/ min.	@ 30°C
T_{TCO}	Maximum charging temperature	-	50	-	°C	High temperature charge termination

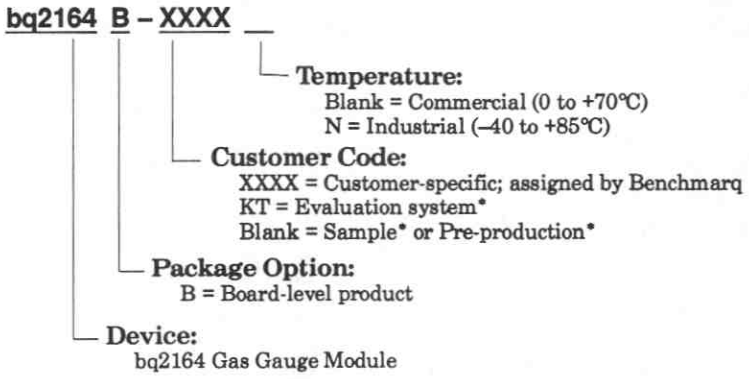
Notes:
1. Default value; value set in DMF register.
2. PVD termination disables the low-temperature fault charge termination.

DC Electrical Characteristics (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit
NumCell	Number of cells in battery pack	5	-	12	-
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]
I_{OL}	Open-drain sink current DQ	-	-	5.0	mA[1]
V_{OL}	Open-drain output low, I_{OL} < 5mA, DQ	-	-	0.5	V[1]
V_{IHDQ}	DQ input high	2.5	-	-	V[1]
V_{IHDQ}	DQ input low	-	-	0.8	V[1]
V_{OS}	Voltage offset			150	µV[1]

Note: 1. Characterized on PCB, IC 100% tested.

Ordering Information



*Requires configuration sheet (see Table 1)

Notes

Preliminary **bq2902**

Rechargeable Alkaline Charge IC

Features

- Safely charges two rechargeable alkaline batteries such as Renewal® from Rayovac®
- Terminates pulsed charge with maximum voltage limit
- Contains LED charge status output
- Features a pin-selectable low-battery cut-off
- Available in 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2902 is a low-cost charger for rechargeable alkaline batteries such as Renewal® batteries from Rayovac®. The bq2902 combines sensitive, full-charge detection for two rechargeable alkaline cells, with a low-battery cut-off for cost-effective battery management.

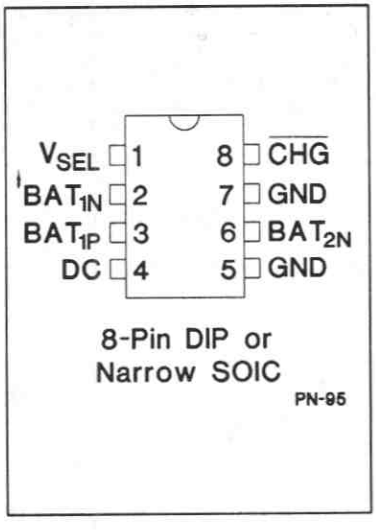
Designed for system integration into a two-cell system, the bq2902 can improve the service life of the rechargeable alkaline cells by properly managing the charge and discharge. The bq2902 uses a current-limited supply to generate the proper charge pulses for the Renewal cell. Each cell is individually monitored to ensure full charge detection without a damaging overcharge.

Charge completion is indicated when the effective charge rate falls below approximately 1/32 of the fast charge rate. Status outputs are provided to indicate charge in progress, charge complete, or fault indication.

The bq2902 avoids over-depleting the battery by using the internal low-battery detection circuit. The bq2902 also eliminates the external power switching transistors needed to separately charge individual Renewal cells.

For safety, charging is inhibited if the per-cell voltage is greater than 3.0V during charge (closed-circuit voltage), or if the cell voltage is less than 0.4V (open-circuit voltage).

Pin Connections



8-Pin DIP or
Narrow SOIC

PN-95

Pin Names

DC	Charging supply input	BAT_{2N}	Battery 2 negative input
$\overline{CHG}$	Battery status output	GND	Charging supply return
BAT_{1P}	Battery 1 positive input	V_{SEL}	End of discharge voltage select input
BAT_{1N}	Battery 1 negative input		

Pin Descriptions

DC **DC supply input**

This input is used to recharge the individual rechargeable alkaline cells and is limited to 5.5V at 300mA.

$\overline{CHG}$ **Charge status**

This open-drain output is used to signify battery charging and is valid only when DC is applied.

V_{SEL} **End-of-discharge select input**

This three-level input selects the desired end-of-discharge cut-off voltage for the bq2902. V_{SEL} = BAT_{1P} selects an EDV of 1.10V. V_{SEL} float selects EDV = 1.0V. V_{SEL} = BAT_{2N} selects EDV = 0.9V

BAT_{1P} **Battery 1 positive input**

This input connects to the positive terminal of the battery designated BAT_1 (see Figure 2).

BAT_{1N} **Battery 1 negative input**

This input connects to the negative terminal of the battery designated BAT_1 (see Figure 2).

BAT_{2N} **Battery 2 negative terminal**

This input connects to the negative terminal of the battery designated BAT_2 (see Figure 2).

GND **Charging supply return**

This input is the DC ground.

Functional Description

Figure 1 illustrates the charge control and display status during a bq2902 cycle. Table 1 outlines the various operational states and their associated conditions which are described in detail in the following section.

Charging

The bq2902 controls the current pulses to properly charge two rechargeable alkaline cells. The charge current is derived from a current-limited DC input and is pulsed at approximately 100 Hz on the BAT_{1P} pin. The DC current input must be limited to less than 5.5V and 300mA.

The bq2902 charge cycle is controlled by inputs from DC and BAT1P . The charge cycle begins with the application of a valid DC input. The bq2902 checks the open-circuit voltage (V_{OCV}) of each cell for an undervoltage condition (V_{MIN} < 0.4V) and begins a charge cycle if V_{OCV} is above V_{MIN}. If V_{OCV} of any cell is below V_{MIN}, the bq2902 enters a charge-pending mode and indicates a fault condition (see Table 1). The bq2902 remains in a charge-pending mode until V_{OCV} of each cell is above V_{MIN}.

The bq2902 charges the rechargeable alkaline battery by pulsing the cells for 7.5ms every 10ms. The bq2902 measures the open circuit voltage (V_{OCV}) of each battery during the idle period. If a single-cell potential of any battery is above the maximum open-circuit voltage (V_{MAX} = 1.63V ± 3%), the following pulses are skipped until the cell potential is below the V_{MAX} limit.

Charging is terminated when the effective charge rate falls below 1/32 of the fast charge rate. Charging is immediately terminated if V_{CCV} (closed-circuit voltage) is greater than 3.0V (V_{FLT}) on any cell during charge. In this case, the $\overline{CHG}$ output is forced to a fault condition (see Table 1). Charging is not re-initiated until either DC is removed and reapplied or V_{OCV} falls below 1.4V.

Low Battery Cut-off

The battery output remains valid until the single-cell voltage of any battery falls below the end-of-discharge voltage selected by the V_{SEL} pin. Table 2 outlines the three EDV selections for the bq2902. If the bq2902 determines an overdischarge condition, the internal switch disconnects the battery from the discharge load.

Charge Status Indication

Table 1 outlines the various action states and the associated $\overline{CHG}$ state. The $\overline{CHG}$ output may be connected directly to an LED indicator as shown in Figure 2. In all cases, if the DC voltage at the DC pin is absent, $\overline{CHG}$ output is held in a high-impedance condition.

2

Table 2. bq2902 EDV Selections

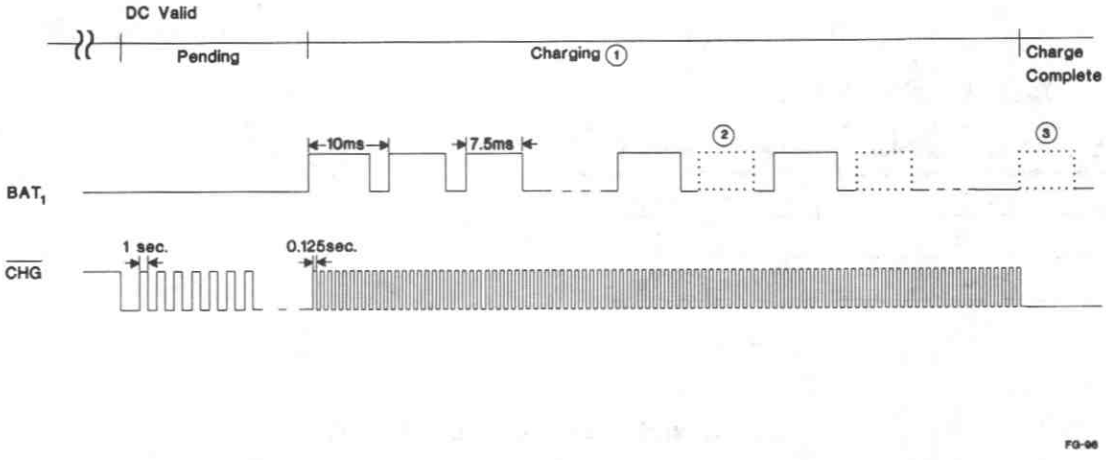
End-of-Discharge Voltage	Pin Connection
1.10V	$V_{SEL} = BAT_{1P}$
1.00V	$V_{SEL} = Z$
0.90V	$V_{SEL} = BAT_{2N}$

Table 1. bq2902 Operational Summary

Charge Action State	Conditions	BAT_{1P} Input	$\overline{CHG}$ Output
DC absent	$V_{DC} = 0$	Low battery detection per V_{SEL}	Z
Charge initiation	DC applied, $V_{OCV} \leq 1.63V$[1]	-	-
Charge pending/ fault	$V_{OCV} < 0.4V$ or $V_{CCV} > 3.0V$[2]	-	1 sec = Low 1 sec = Z
Fast charging	$V_{OCV} \leq 1.63V$ before pulse	Charge pulsed @ 100Hz per Figure 1	1/8 sec = Low 1/8 sec = Z
Pulse skip	V_{OCV} remains above 1.63V during pulse cycle	Pulse skipped per Figure 1	1/8 sec = Low 1/8 sec = Z
Charge complete	Charge rate falls below 1/32 of the fast charge rate	Charge complete	Low

Notes: 1. V_{OCV} = Open-circuit voltage of each cell between positive and negative leads.

2. V_{CCV} = Closed-circuit voltage.



Notes:

1. **Charging: $0.4 < V_{OCV} \leq 1.63V$, $V_{CCV} \leq 3.0V$.**
2. **Pulses skipped when $V_{OCV} > 1.63V$.**
3. **Charge complete when charge falls below 1/32 of fast charge rate**

Figure 1. bq2902 Application Diagram

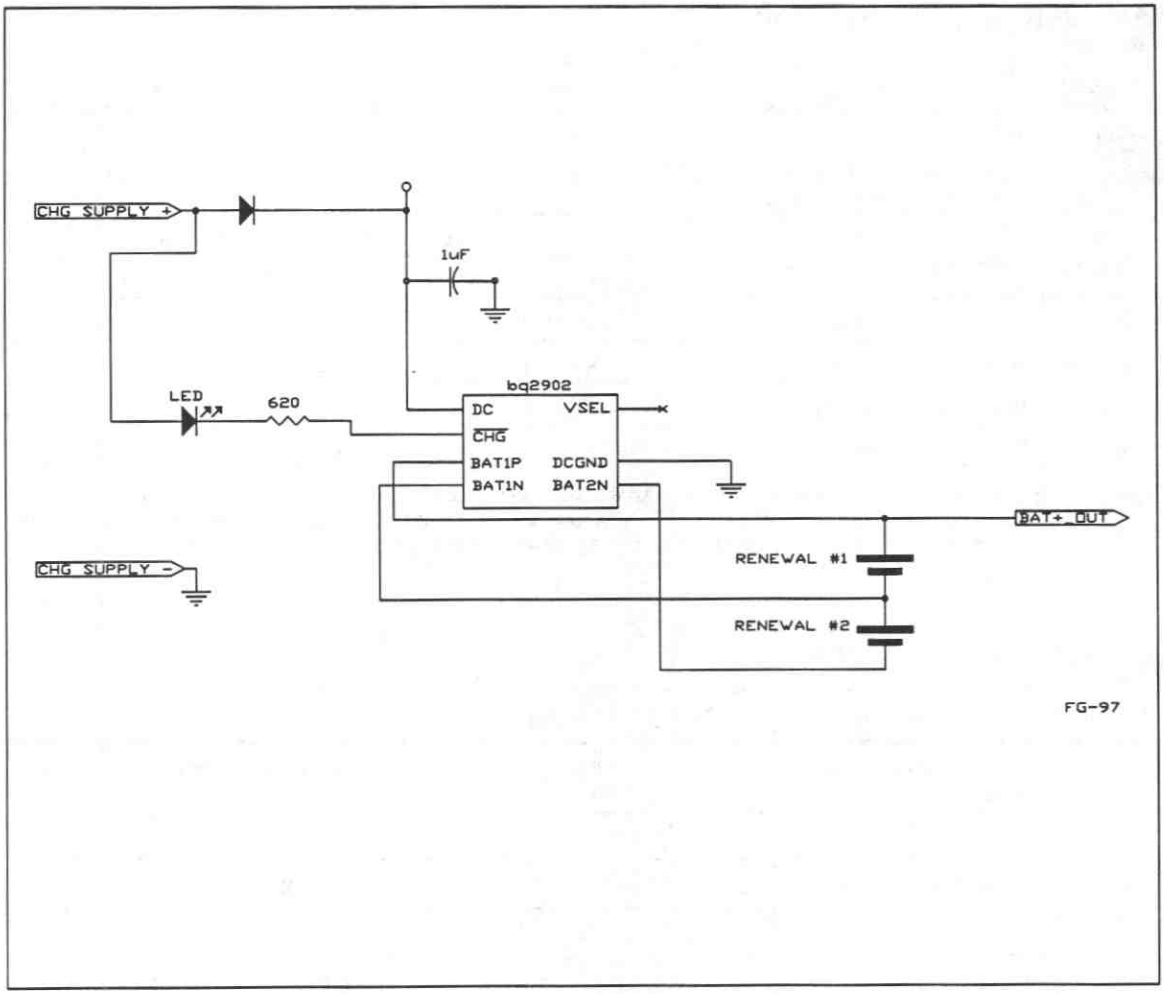


Figure 2. bq2902 Application Example

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
DC_{IN}	V_{DC} relative to V_{SS}	-0.3	11.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	11.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	
I_{DC}	DC charging current	-	400	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{DC} = 5.5V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{MAX}	Maximum open-circuit voltage	1.63	±3%	V	$V_{OCV} > V_{MAX}$ inhibits/terminates charge pulses
V_{EDV}	End-of-discharge voltage	0.90V	±5%	V	$V_{SEL} = BAT_{2N}$
		1.0V	±5%	V	$V_{SEL} = Z$
		1.10V	±5%	V	$V_{SEL} = BAT_{1P}$
V_{FLT}	Maximum open-circuit voltage	3V	±3%	V	$V_{CCV} > V_{FLT}$ terminates charge, indicates fault
V_{MIN}	Minimum battery voltage	0.4V	±3%	V	$V_{OCV} < V_{MIN}$ inhibits charge

Recommended DC Operating Conditions (T_A = T_{OPR})

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{IH}	Logic input high	V_{DC} - 0.5	-	-	V	V_{SEL}
V_{IL}	Logic input low	-	-	0.5	V	V_{SEL}
V_{OL}	Logic output low	-	-	0.8	V	$\overline{CHG}$, I_{OL} = 10mA
I_{OL}	Output current	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V, $\overline{CHG}$
I_{CC}	Supply current	-	-	250	µA	Outputs unloaded, V_{DC} = 5.5V
I_{SB1}	Standby current	-	-	10	µA	V_{DC} = 0, V_{OCV} > V_{MIN}
I_{SB2}	End-of-discharge standby current	-	-	1	µA	
I_L	Input leakage	-	-	±1	µA	V_{SEL}
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{CHG}$
R_{DSON}	On resistance	-	0.5	-	Ω	
I_{IL}	Logic input low	-	-	70	µA	V_{SEL}
I_{IH}	Logic input high	-70	-	-	µA	V_{SEL}
I_{IZ}	Logic input float	-2	-	2	µA	V_{SEL}
I_{DC}	DC charging current	-	-	300	mA	
V_{DC}	DC charging voltage	3.3V	-	5.5	V	

Note: All voltages relative to GND.

Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_P	Pulse timer	-	100	-	Hz	See Figure 3
t_{PW}	Pulse width	-	7.5	-	ms	See Figure 3

Note: Typical is at $T_A = 25°C$.

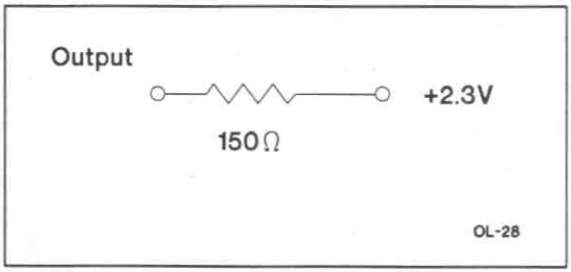


Figure 3. Output Load

Ordering Information

bq2902 _ _

- Temperature Range:
  - blank = Commercial (-20 to +70°C)
  - N = Industrial (-40 to +85°C)
- Package Option:
  - PN = 8-pin narrow plastic DIP
  - SN = 8-pin narrow SOIC
- Device:
  - bq2902 Rechargeable Alkaline Charge IC

BENCHMARQ

Preliminary **bq2903**

Rechargeable Alkaline Charge IC

Features

- Safe charge of three or four rechargeable alkaline batteries such as Renewal® from Rayovac®
- Pulsed charge terminated with maximum voltage limit
- LED outputs indicate charge status
- Selectable end-of-discharge voltage prevents overdischarge and improves cycle life
- Optional external FET drive allows high current loads
- Pre-charge qualification indicates fault conditions
- Automatic charge control simplifies charger design
- 14-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2903 is a cost-effective charge controller for rechargeable alkaline batteries such as Renewal® batteries from Rayovac®. The bq2903 combines sensitive, full-charge detection for three to four rechargeable alkaline cells, with a low-battery cut-off for cost-effective battery management.

Designed for integration into a three- to four-cell system, the bq2903 can improve the service life of the rechargeable alkaline cells by properly managing the charge and discharge cycles. The bq2903 uses a current-limited supply to generate the proper charge pulses for the Renewal® cell. Each cell is individually monitored to ensure full charge detection without a damaging overcharge.

Charge completion is indicated when the effective charge rate falls below approximately 3% of the fast charge rate. Status outputs are provided to indicate charge in progress, charge complete, or fault condition.

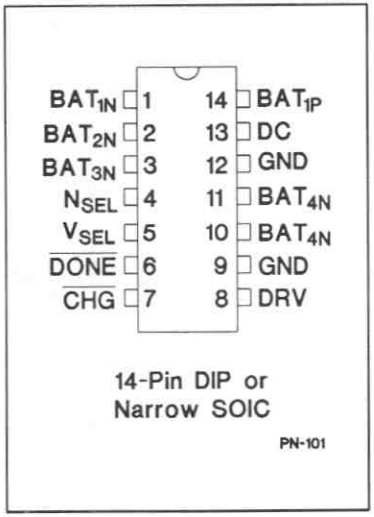
The bq2903 avoids over-depleting the battery by using the internal end-of-discharge control circuitry. The bq2903 also eliminates the external power switching transistors needed to separately charge individual Renewal® cells.

To reduce cost, the discharge and charge control FETs are internal to the bq2903. An optional DRV pin is provided to drive an external N-FET, reducing the effective R_{DSON} for the system, if needed.

For safety, charging is inhibited if the voltage of any cell is greater than 3.0V during charge or if the voltage of any cell is less than 0.4V when not charging (open-circuit voltage).

2

Pin Connections



14-Pin DIP or
Narrow SOIC

PN-101

Pin Names

DC	Charging supply input	BAT_{1N}	Battery 1 negative input
$\overline{CHG}$	Battery status output 1	BAT_{2N}	Battery 2 negative input
$\overline{DONE}$	Battery status output 2	BAT_{3N}	Battery 3 negative input
N_{SEL}	Number of cells input	BAT_{4N}	Battery 4 negative input
V_{SEL}	End of discharge voltage select input	GND	Charging supply return
		DRV	External FET drive output
BAT_{1P}	Battery 1 positive input		

Pin Descriptions

DC **DC supply input**

This input is used to recharge the rechargeable alkaline cells and power the bq2903 during charge. This input must be limited to 10V and 300mA.

$\overline{CHG}$ **Charge status**

This open-drain output is used to signify the battery charging status and is valid only when DC is applied. See Figure 1 and Table 1.

$\overline{DONE}$ **Charge done**

This open-drain output is used to signify charge completion and is valid only when DC is applied.

N_{SEL} **Number of cells input**

This input selects whether the bq2903 charges 3 or 4 cells. N_{SEL} = BAT_{1P} selects 4 cells, and N_{SEL} = BAT_{4N} selects 3 cells.

V_{SEL} **End-of-discharge select input**

This three-level input selects the desired end-of-discharge cut-off voltage for the bq2903. V_{SEL} = BAT_{1P} selects an EDV of 1.10V. V_{SEL} floating selects EDV = 1.0V. V_{SEL} = BAT_{4N} selects EDV = 0.9V.

BAT_{1P} **Battery 1 positive input**

This input connects to the positive terminal of the battery designated BAT_1 (see Figure 2). This pin also provides power to the bq2903 when DC is not present.

BAT_{1N} **Battery 1 negative input**

This input connects to the negative terminal of the battery designated BAT_1 (see Figure 2).

BAT_{2N} **Battery 2 negative terminal**

This input connects to the negative terminal of the battery designated BAT_2 (see Figure 2).

BAT_{3N} **Battery 3 negative terminal**

This input connects to the negative terminal of the battery designated BAT_3 (see Figure 2).

BAT_{4N} **Battery 4 negative terminal**

This input connects to the negative terminal of the battery designated BAT_4 (see Figure 2).

GND **Charging supply return**

This input is the DC ground.

DRV **External FET drive output**

This push-pull output drives an optional external N-FET on the ground side of the battery stack (see Figure 2). This pin should not be connected if the external FET is not used. See page 5 for a full description.

NC **No connect**

Functional Description

Figure 1 illustrates the charge control and display status during a bq2903 cycle. Table 1 outlines the various operational states and their associated conditions which are described in detail in the following section.

Charge Action Control

The bq2903 initiates a charge cycle when a valid DC input is applied or if all the cells fall below 1.4V after a completed charge cycle. The DC input should be capable of supplying a minimum of 2.0V * N where N is the number of cells to be charged, either 3 or 4. The DC current must be limited to 300mA.

Once a charge cycle begins, the bq2903 terminates charge when the charge rate falls below 3% of the maximum charge rate. The bq2903 also terminates charge when the voltage of any cell exceeds 3.0V during charge, which indicates a fault condition.

Charge Status Indication

Table 1 and Figure 1 outline the various charge action states and the associated BAT_{1P}, $\overline{CHG}$, and $\overline{DONE}$ output states. The charge status outputs are designed to work with individual or tri-color LED indicators. In all cases, if the DC pin is not valid, $\overline{CHG}$ and $\overline{DONE}$ outputs are held in a high-impedance condition.

Fast-Charge Prequalification

After DC is valid, and prior to charge, the bq2903 checks the open-circuit voltage (V_{OCV}) of each cell for an undervoltage condition (V_{MIN} < 0.4V) and begins a charge cycle if V_{OCV} is above V_{MIN}. If V_{OCV} of any cell is below V_{MIN}, the bq2903 enters a charge-pending mode and indicates a fault condition (see Table 1). The bq2903 remains in a charge-pending mode until V_{OCV} of each cell is above V_{MIN}.

Charging

The bq2903 controls the charge by periodically switching a current-limited DC supply to the battery stack. The charge current is delivered from a current-limited DC supply and is pulsed at approximately 100 Hz on the BAT_{1P} pin. The DC input must be limited to less than 10V and 300mA.

The bq2903 pulse charges the battery for approximately 7.5ms of every 10ms, when conditions warrant. The bq2903 measures the open circuit voltage (V_{OCV}) of each battery during the idle period. If a single-cell potential of any battery is above the maximum open-circuit voltage (V_{MAX} = 1.63V ± 3%), the following pulses are skipped until all cell potentials fall below the V_{MAX} limit. Charging is immediately terminated if V_{CCV} (closed-circuit voltage) is greater than 3.0V (V_{FLT}) on any cell and the $\overline{CHG}$ output indicates a fault condition (see Table 1).

Charging is terminated when the effective charge rate falls below approximately 3% of the maximum charge

Table 1. bq2903 Operational Summary

Charge Action State	Conditions	BAT_{1P} Input	$\overline{CHG}$ Output	$\overline{DONE}$ Output
DC absent	$V_{DC} < V_{BAT1P}$	Low battery detection per V_{SEL}	Z	Z
Charge initiation	DC applied, $V_{OCV} \leq 1.63V$[1]	-	-	-
Charge pending/ fault	$V_{OCV} < 0.4V$ or $V_{CCV} > 3.0V$[2]	-	1/6 sec = Low 1/6 sec = Z	Z
Fast charging	$V_{OCV} \leq 1.63V$ before pulse	Charge pulsed @ 100Hz per Figure 1	Low	Z
Pulse skip	V_{OCV} remains above 1.63V during pulse cycle	Pulse skipped per Figure 1	Low	Z
Charge complete	Charge rate falls below 3% of the fast charge rate	Charge complete	Z	Low

Notes: 1. V_{OCV} = Open-circuit voltage of each cell between positive and negative leads.

2. V_{CCV} = Closed-circuit voltage.

rate. Once charging is terminated, the $\overline{\text{DONE}}$ output becomes active per Table 1 and Figure 1.

Trickle Charge/Charge Re-Initiation

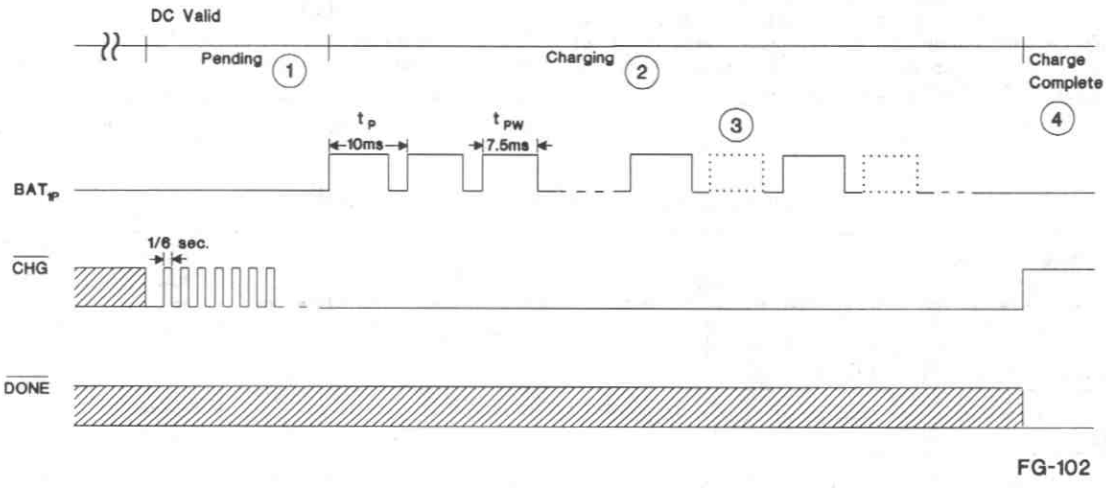
The rechargeable alkaline cells, unlike other rechargeable chemistries, do not require a maintenance charge to keep the cells in a fully charged state. The self-discharge rate for the Renewal® cells is typically 4% per year at room temperature. The bq2903 always initiates a charge cycle when DC is first applied. If DC remains valid, the bq2903 suspends all charge activity after full-charge termination until V_{OCV} of all the cells falls below 1.4V. At this time, the bq2903 begins a new charge cycle.

End-of-Discharge Control

During discharge, the bq2903 monitors the cell voltage of the rechargeable alkaline cells. This limits the individual cell discharge voltage and improves the cycle performance. If the voltage across any cell is below the voltage specified by the V_{SEL} input, the bq2903 disconnects the battery stack from the load. The DRV output is also driven low, disabling the external FET. This discharge voltage limit is pin-selectable between 1.1, 1.0, and 0.9 volts as outlined in Table 2. Typically, higher

Table 2. bq2903 EOD Voltage Selections

End-of-Discharge Voltage	Pin Connection
1.10V	$V_{SEL} = BAT_{1P}$
1.00V	$V_{SEL} = Z$
0.90V	$V_{SEL} = BAT_{4N}$



Notes:
1. Charge Pending = $V_{OCV} < 0.4V$ per cell, $V_{CCV} > 3.0V$ per cell.
2. Charging: $0.4 < V_{OCV} \leq 1.63V$, $V_{CCV} \leq 3.0V$.
3. Pulses skipped when $V_{OCV} > 1.63V$.
4. Charge complete when charge rate falls below approximately 3% of the fast charge rate.

Figure 1. bq2903 Example of Charge Action Events

discharge loads (>200mA) should use a lower discharge voltage cut-off.

The bq2903 maintains the discharge cut-off until the batteries are replaced or DC becomes valid, initiating a new charge cycle. During the discharge cut-off, the standby current in the bq2903 is reduced to less than 1µA.

Number-of-Cell Selection

N_{SEL} is used to select whether the bq2903 charges 3 or 4 cells. Figure 2 shows the proper connection for a 3- or 4-cell system. N_{SEL} = BAT_{1P} selects 4 cells. NSEL = BAT_{4N} selects 3 cells. BAT_{2N} should be connected to BAT_{3N} in this case.

DRV Pin

The bq2903 controls charge using internal switches between the DC input and BAT_{1P}, and between BAT_{4N} and GND. During charge, this current should be limited to 300mA. During discharge, the bq2903 controls an internal switch between BAT_{4N} and GND. This switch is limited to 400mA. To reduce the series resistance associated with the discharge switch, or for high current loads, the bq2903 provides an external DRV pin which can be used to control an optional N-FET, as shown in Figure 3. When enabled, DRV is internally pulled up to DC or BAT_{1P}, turning the FET on during charge and discharge. DRV is driven low to turn off the external FET to protect the battery from deep discharge. This pin should not be connected if the external FET option is not used.

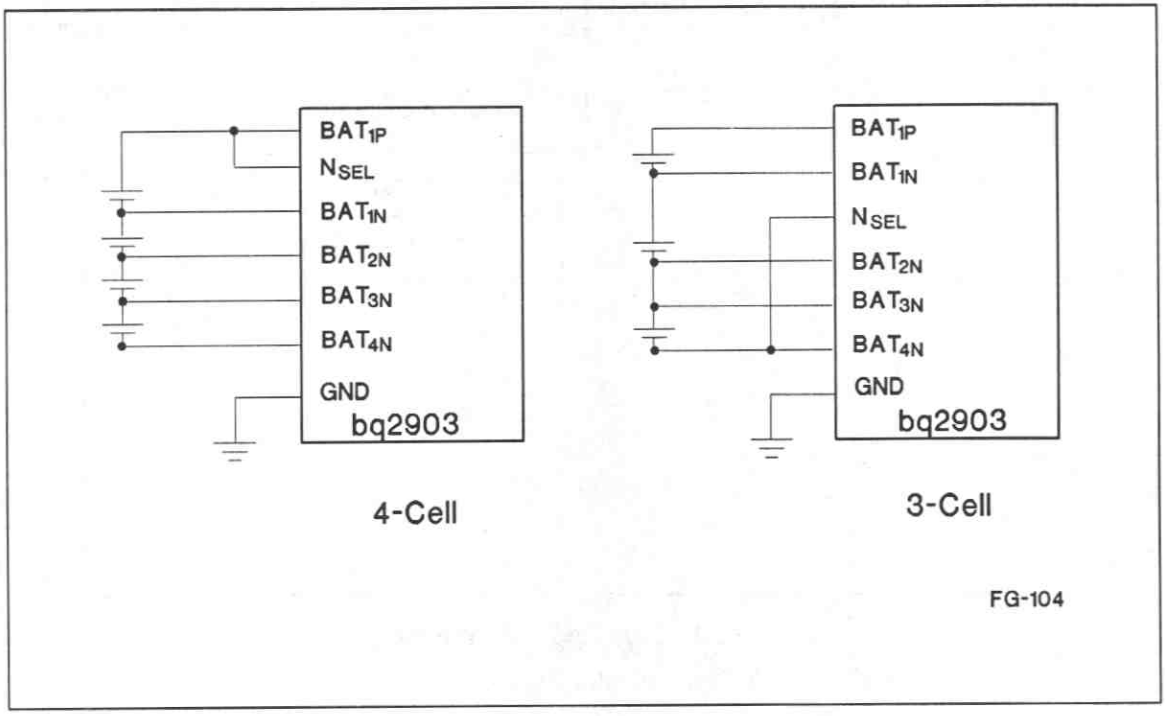


Figure 2. N_{SEL} Connection Diagram

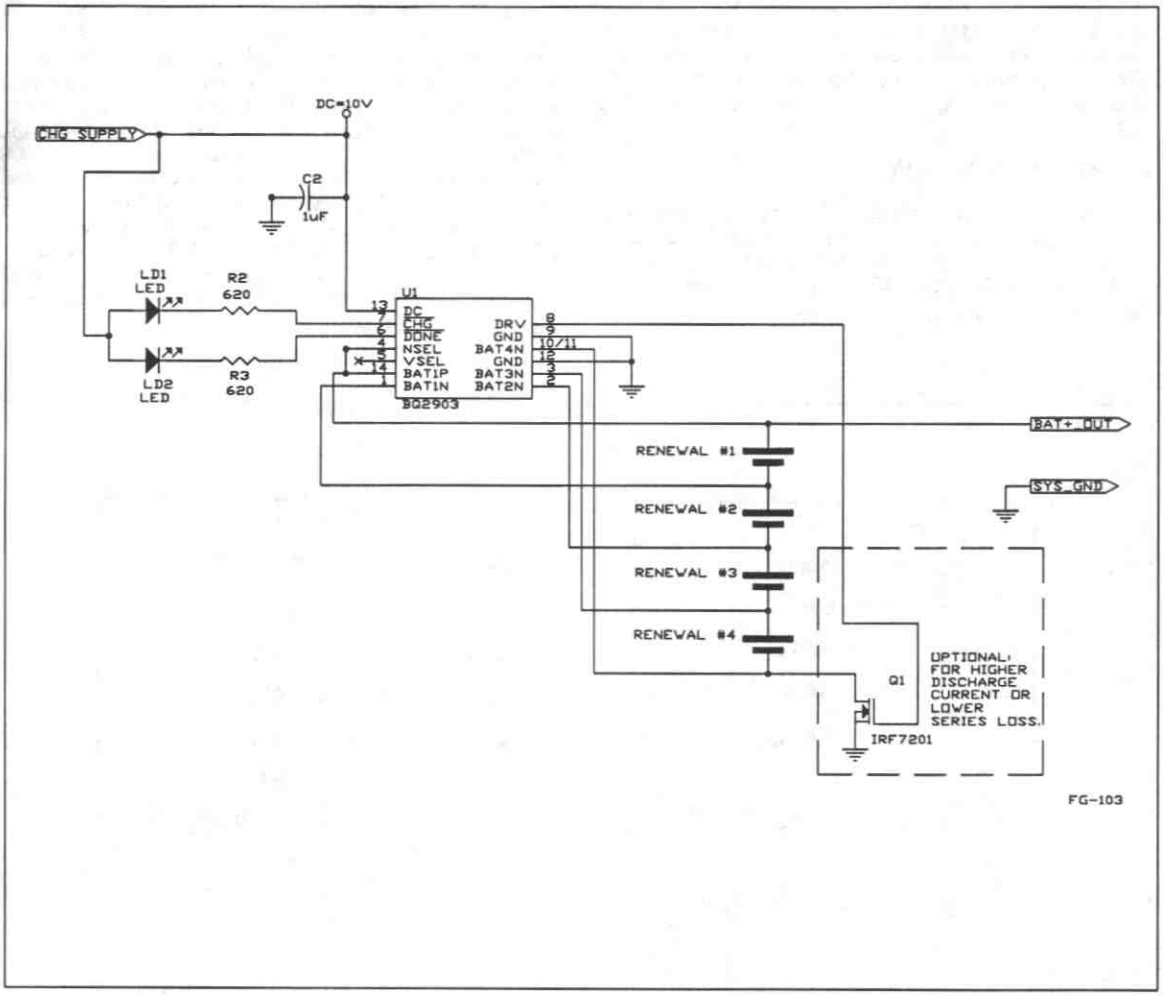


Figure 3. bq2903 Application Example, 4–Cell and 1.0V EOD Limit

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
DC_{IN}	V_{DC} relative to V_{SS}	-0.3	11.0	V	
V_T	DC voltage applied on any pin excluding DC relative to V_{SS}	-0.3	11.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	
I_{DC}	DC charging current	-	400	mA	
I_{LOAD}	Discharge current	-	500	mA	No external FET

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{DC} = 10V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{MAX}	Maximum open-circuit voltage	1.63	±3%	V	$V_{OCV} > V_{MAX}$ inhibits or terminates charge pulses
V_{EDV}	End-of-discharge voltage	0.90V	±5%	V	$V_{SEL} = BAT_{4N}$
		1.0V	±5%	V	$V_{SEL} = Z$
		1.10V	±5%	V	$V_{SEL} = BAT_{1P}$
V_{FLT}	Maximum closed-circuit voltage	3V	±5%	V	$V_{CCV} > V_{FLT}$ terminates charge, indicates fault
V_{MIN}	Minimum battery voltage	0.4V	±5%	V	$V_{OCV} < V_{MIN}$ inhibits charge
V_{CE}	Charge enable	1.4V	±5%	V	$V_{OCV} < V_{CE}$ on all cells re-initiates charge

Recommended DC Operating Conditions (T_A = T_{OPR})

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{IH}	Logic input high	V_{DC} - 0.5	-	-	V	V_{SEL}, N_{SEL}
V_{IL}	Logic input low	-	-	0.5	V	V_{SEL}, N_{SEL}
V_{OL}	Logic output low	-	-	1.0	V	$\overline{DONE}$, $\overline{CHG}$, I_{OL} = 5mA
		-	-	0.4	V	I_{OL} = 1.0mA, DRV
V_{OH}	Gate drive output	(Greater of BAT_{1P} or DC) - 0.8	-	-	V	DRV, I_{OH} = -1.0mA
I_{OL}	Output current	5	-	-	mA	V_{OL} = V_{SS} + 1.0V, $\overline{CHG}$, $\overline{DONE}$, DRV
I_{DC}	Supply current	-	-	250	µA	Outputs unloaded, V_{DC} = 10.0V
I_{SB1}	Standby current	-	-	25	µA	V_{DC} = 0, V_{OCV} > V_{MIN}, BAT_{1P-3N}
I_{SB2}	End-of-discharge standby current	-	-	1	µA	V_{DRV} = 0V, V_{DC} < 6.5V
I_L	Input leakage	-	-	±1	µA	NSEL
I_{OZ}	Output leakage in high-Z state	-	-	±5	µA	$\overline{CHG}$, $\overline{DONE}$
R_{DSON}	Discharge on resistance	-	0.5	-	Ω	
I_{LOAD}	Discharge current without external N-FET	-	-	400	mA	No external FET
I_{IL}	Logic input low	-	-	70	µA	V= V_{SS} to V_{SS} + 0.5V, V_{SEL}
I_{IH}	Logic input high	-70	-	-	µA	V = V_{DC} -0.5 to V_{DC}, V_{SEL}
I_{IZ}	Logic input float	-2	-	2	µA	V_{SEL}
I_{DC}	DC charging current	-	-	300	mA	
V_{DC}	DC charging voltage	2.0 * number of cells	-	10	V	

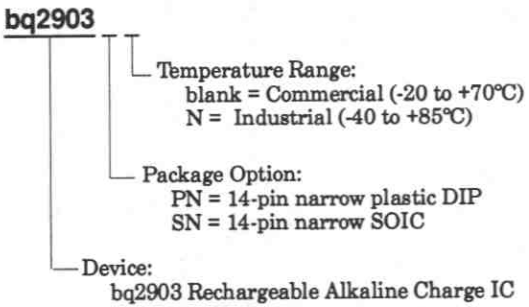
Note: All voltages relative to GND.

Timing (TA = TOPR, Refer to Figure 1)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_P	Pulse period	-	10	-	ms	See Figure 1
t_{PW}	Pulse width	-	7.5	-	ms	See Figure 1

Note: Typical is at $T_A = 25°C$.

Ordering Information



Notes

BENCHMARQ

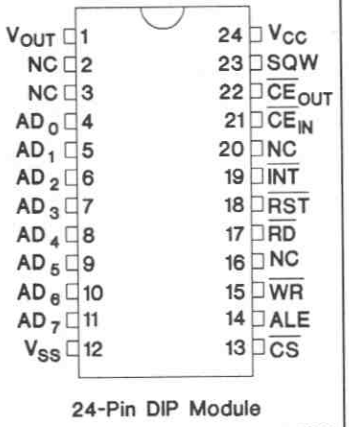
bq4287E

Enhanced RTC Module With NVRAM Control

Features

- Enhanced features include:
  - System wake-up capability—alarm interrupt output active in battery-backup mode
  - 32kHz output for power management
- 114 bytes of general nonvolatile storage
- Automatic backup and write-protect control to external SRAM
- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Integral lithium cell and crystal in 24-pin DIP module
- 160 ns cycle time allows fast bus operation
- Better than one minute per month clock accuracy
- Less than 0.5 µA load under battery operation
- Intel bus timing
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122 µs to 500 ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle

Pin Connections



24-Pin DIP Module

PN-29

Pin Names

AD0–AD7	Multiplexed address/data input/output
$\overline{CS}$	Chip select input
ALE	Address strobe input
$\overline{RD}$	Data strobe input
$\overline{WR}$	Read/write input
$\overline{INT}$	Interrupt request output
$\overline{RST}$	Reset input
SQW	Square wave output
$\overline{CE}_{IN}$	RAM chip enable input
$\overline{CE}_{OUT}$	RAM chip enable output
NC	No connect
VOUT	Supply output
VCC	+5V supply
VSS	Ground

General Description

The CMOS bq4287E is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. Other features include three maskable interrupt sources, square wave output, and 114 bytes of general nonvolatile storage.

A 32.768kHz output is available for sustaining power-management activities. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode.

The bq4287E write-protects the clock, calendar, and storage registers during power failure. The integral backup energy source then maintains data and operates the clock and calendar.

The bq4287E is a fully compatible real-time clock for IBM AT-compatible computers and other applications.

The bq4287E integrates a battery-backup controller and battery to make a standard CMOS SRAM nonvolatile during power-fail conditions. During power-fail, the bq4287E automatically write-protects the external SRAM and provides a VCC output sourced from its internal battery.

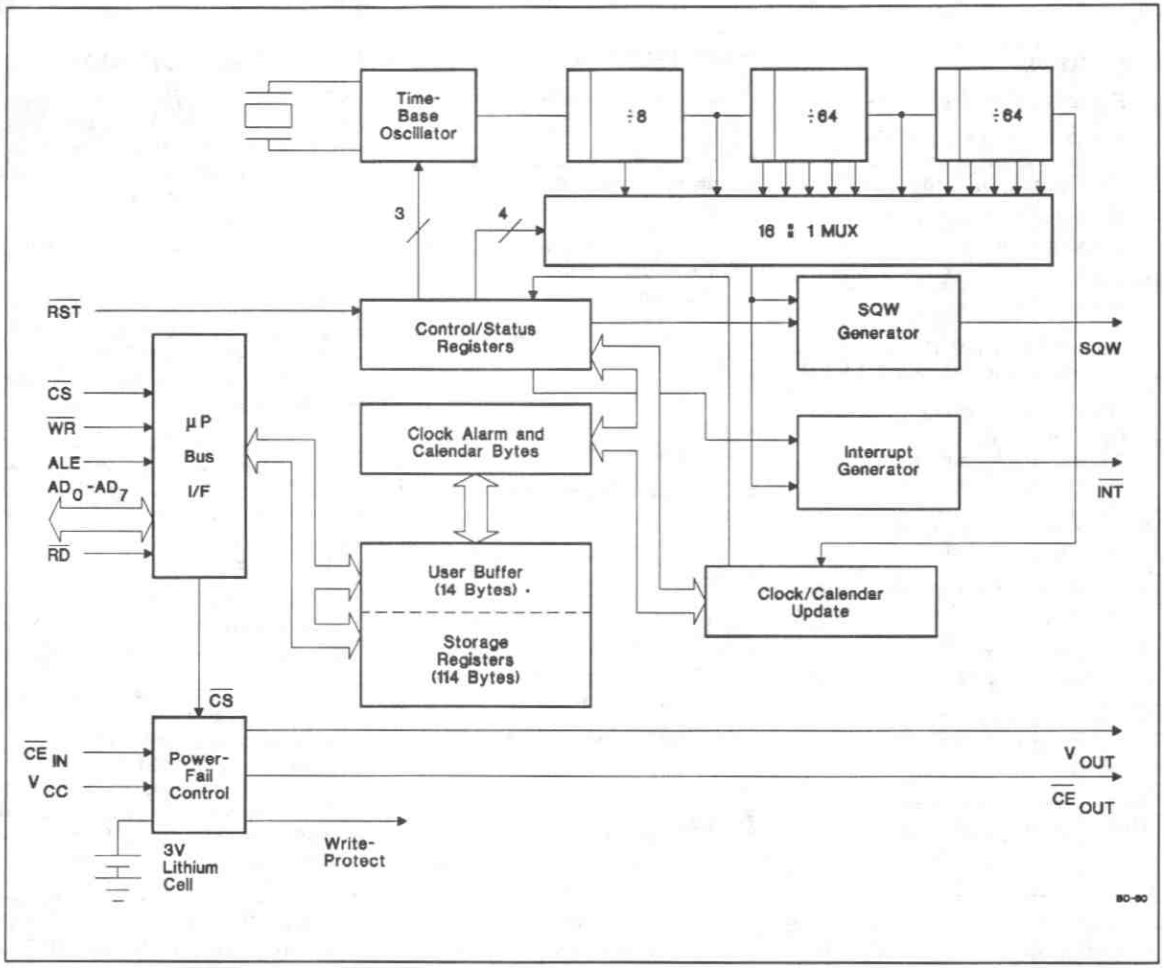
As shipped from Benchmarq, the backup cell is electrically isolated from the memory. Following the first application of VCC, this isolation is broken, and the backup cell provides data retention to the clock, internal RAM, VOUT, and $\overline{CE}_{OUT}$ on subsequent power-downs.

Caution:

Care should be taken to avoid inadvertent discharge through VOUT and $\overline{CE}_{OUT}$ after battery isolation has been broken.

4

Block Diagram



Pin Descriptions

AD_0–AD_7 **Multiplexed address/data input/output**

The bq4287E bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 is latched into the bq4287E on the falling edge of the ALE signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins act as a bidirectional data bus.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq4287E.

ALE **Address latch enable**

ALE serves to demultiplex the address/data bus. The falling edge of ALE latches the address on AD_0–AD_7. This demultiplexing process is independent of the $\overline{CS}$ signal.

$\overline{RD}$ **Read input**

The falling edge on $\overline{RD}$ is used to enable the outputs during a read cycle.

$\overline{WR}$ **Write input**

The rising edge on $\overline{WR}$ latches data into the bq4287E.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. This allows INT to be valid in battery-backup mode for the alarm interrupt. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

$\overline{RST}$ **Reset input**

The bq4287E is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high-impedance, and the bq4287E is not accessible. Table 3 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

SQW **Square-wave output**

SQW may output a programmable frequency square-wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

A 32.768kHz output is enabled by setting the SQWE bit in register B to 1 and the 32KE bit in register C to 1 after setting OSC2–OSC0 in register A to 011 (binary).

$\overline{CE_{IN}}$ **External RAM chip enable input, active low**

$\overline{CE_{IN}}$ should be driven low to enable the controlled external RAM. $\overline{CE_{IN}}$ is internally pulled up with a 50KΩ resistor. $\overline{CE_{IN}}$ is internally pulled up with a 50KΩ resistor.

$\overline{CE_{OUT}}$ **External RAM chip enable output, active low**

When power is valid, $\overline{CE_{OUT}}$ reflects $\overline{CE_{IN}}$.

V_{OUT} **Supply output**

V_{OUT} provides the higher of V_{CC} or V_{BC}, switched internally to supply external RAM.

V_{CC} **+5V supply**

V_{SS} **Ground**

Functional Description

Address Map

The bq4287E provides 14 bytes of clock and control/status registers and 114 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq4287E.

Update Period

The update period for the bq4287E is one second. The bq4287E updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq4287E copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes is frozen, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

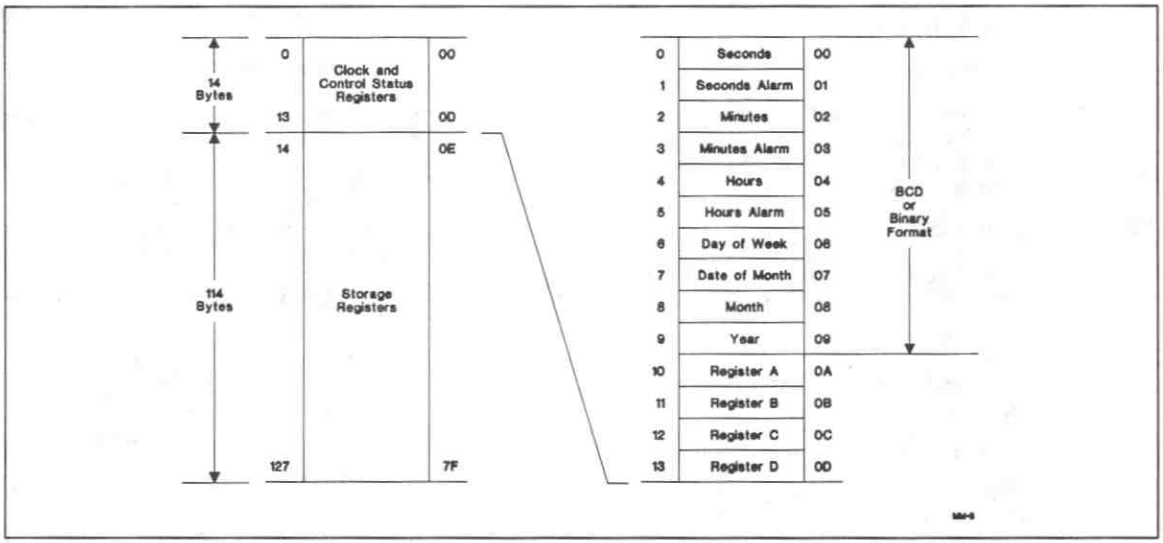


Figure 1. Address Map

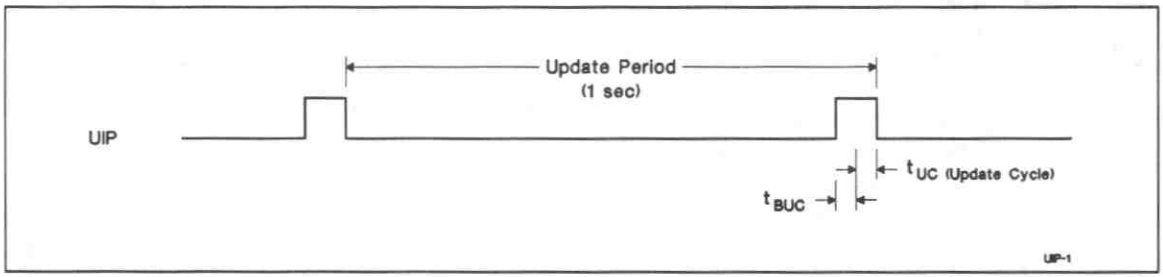


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 1).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format bit (DF) to select BCD or binary format for all clock and calendar bytes.
   c. Write the appropriate value to the hour format bit (HR).
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 1. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–0CH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square-Wave Output

The bq4287E divides the 32.768 kHz oscillator frequency to produce the 1 Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 2). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B. A 32.768kHz output may be selected by setting OSC2–OSC0 in register A to 011 while SQWE = 1 and 32KE = 1.

Interrupts

The bq4287E allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122 µs to 500 ms
- The alarm interrupt, programmable to occur once per second to once per day
- The update-ended interrupt, which occurs at the end of an RTC update cycle

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes $\overline{INT}$ high-impedance.

Two methods can be used to process bq4287E interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 2. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits							Square Wave		Periodic Interrupt	
OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	1	0	0	0	0	0	None		None	
0	1	0	0	0	0	1	256	Hz	3.90625	ms
0	1	0	0	0	1	0	128	Hz	7.8125	ms
0	1	0	0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	1	0	0	4.096	kHz	244.141	µs
0	1	0	0	1	0	1	2.048	kHz	488.281	µs
0	1	0	0	1	1	0	1.024	kHz	976.5625	µs
0	1	0	0	1	1	1	512	Hz	1.953125	ms
0	1	0	1	0	0	0	256	Hz	3.90625	ms
0	1	0	1	0	0	1	128	Hz	7.8125	ms
0	1	0	1	0	1	0	64	Hz	15.625	ms
0	1	0	1	0	1	1	32	Hz	31.25	ms

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 2). Setting OSC2–OSC0 in register A to 011 does not affect the periodic interrupt timing.

Alarm Interrupt

The alarm interrupt request is valid in battery-backup mode, providing a "wake-up" capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar readings during an update cycle may be in error. Three methods to access the RTC bytes without ambiguity are available:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler finishes accessing the clock bytes in $t_{PI}/2 + t_{BUC}$ time (see Figure 3).

Oscillator Control

The bq4287E is shipped from Benchmarq with its internal oscillator turned off. The internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

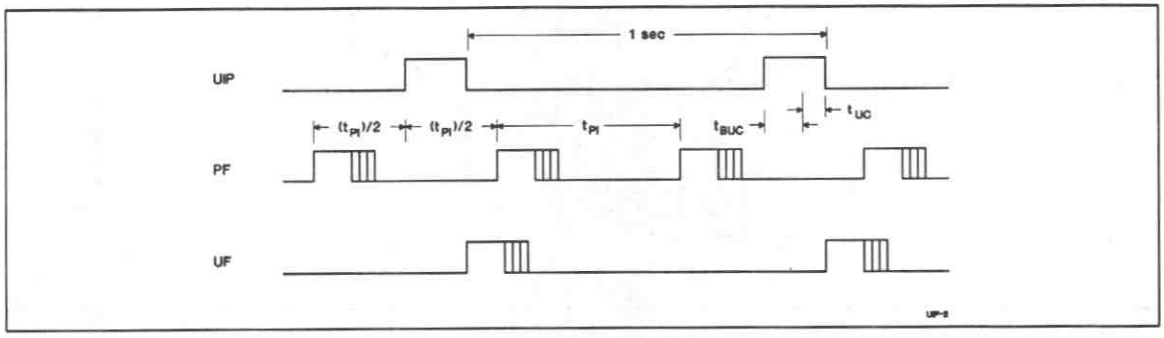


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq4287E continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq4287E write-protects the clock and storage registers. When V_{CC} is below V_{SO} (3V typical), the power source is switched to the internal lithium cell. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{SO}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

An external CMOS static RAM can be battery-backed using the V_{OUT} and RAM chip enable output pins from the bq4287E. As the voltage input V_{CC} slews down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input, $\overline{CE}_{IN}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in process to the external SRAM during power-fail detection, the memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (30µs maximum), the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the internal backup energy source. $\overline{CE}_{OUT}$ is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. $\overline{CE}_{OUT}$ is held inactive for time t_{CER} (200ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}_{IN}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}_{IN}$ input is passed through to the $\overline{CE}_{OUT}$ output with a propagation delay of less than 10 ns.

The internal lithium cell is capable of supplying 3V on V_{OUT} for an extended period of time. The length of time that the external SRAM retains data is a function of the data-retention current of the SRAMs used. The initial capacity of the internal lithium cell is 130mAh. Typically, if the data-retention current for external SRAM is 1µA at room temperature and the clock data-retention current (I_{CCB}) is 0.5µA, cumulative data-retention time is calculated to be more than nine years.

The bq4287E battery life is a function of the time spent in battery-backed mode and the data-retention current of the external SRAM. For example, office equipment is generally powered on for 8 hours and powered off for 16 hours. Under these conditions, a single bq4287E provides an SRAM drawing 1µA total data-retention current with more than 14 years of nonvolatility.

The hardware hookup is shown in Figure 4.

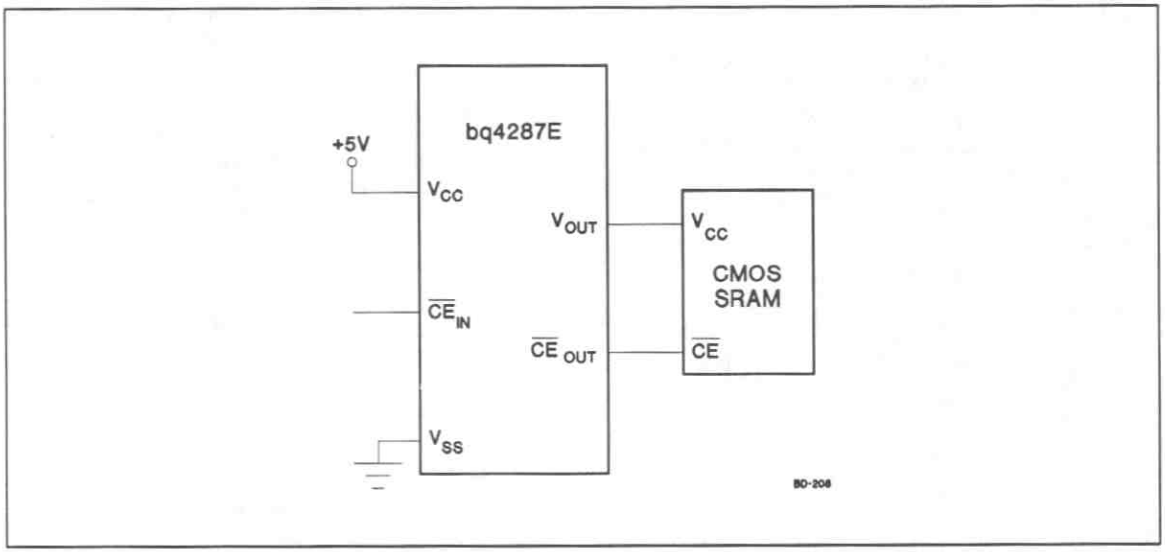


Figure 4. External RAM Hookup to the bq4287E RTC

As shipped from Benchmarq, the internal lithium cell is electrically isolated from V_{OUT} and $\overline{CE}_{OUT}$. Self-discharge in this condition is less than 0.5% per year at 20°C.

Note: Following the first application of V_{CC} above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{CE}_{OUT}$ for the external SRAM.

Caution:

Care should be taken to avoid inadvertent discharge through V_{OUT} and $\overline{CE}_{OUT}$ after battery isolation has been broken.

Control/Status Registers

The four control/status registers of the bq4287E are accessible regardless of the status of the update cycle (see Table 3).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 2.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. The bq4287E is shipped from Benchmarq with its oscillator turned off. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 3. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No[2]	INTF	0	PF	0	AF	0	UF	0	-	0	32KE	na	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.

1. Except bit 7.
2. Read/write only when OSC2–OSC0 in register A is 011 (binary).

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq4287E increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	32KE	0	0

Register C is the read-only event status register.

Bits 0–3 - Unused Bits

7	6	5	4	3	2	1	0
-	-	-	-	0	0	0	0

These bits are always set to 0.

32KE - 32kHz Enable Output

7	6	5	4	3	2	1	0
-	-	-	-	-	32KE	-	-

This bit may be set to a 1 only when the OSC2–OSC0 bits in register A are set to 011. Setting OSC2–OSC0 to anything other than 011 clears this bit. When OSC2–OSC0 are set to 011 and SQWE in register B and 32KE are set, then a 32.768kHz waveform is output on the square wave pin.

UF - Update-Event Flag

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

This bit is set to a 1 at the end of the update cycle. Reading register C clears this bit.

AF - Alarm Event Flag

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

PF - Periodic Event Flag

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

INTF - Interrupt Request Flag

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

These bits are always set to 0.

VRT - Valid RAM and Time

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

1 = Valid backup energy source

0 = Backup energy source is depleted

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-40 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{BIAS}	Temperature under bias	-10 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics (T_A = TOPR, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
C	Battery capacity	-	130	-	mAh	Refer to graphs in Typical Battery Characteristics section
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$ and SQW in high impedance
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$
I_{CCSB}	Standby supply current	-	300	-	µA	V_{IN} = V_{CC} or V_{SS}, $\overline{CS}$ = $\overline{CE}_{IN}$ ≥ V_{CC} - 0.2, no load on V_{OUT}
V_{SO}	Supply switch-over voltage	-	3.0	-	V	
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
V_{BC}	Backup cell voltage	-	3.0	-	V	Internal backup cell voltage; refer to graphs in Typical Battery Characteristics section
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	I_{OUT} = 100mA, V_{CC} > V_{BC}
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V	-	-	V	I_{OUT} = 100µA, V_{CC} < V_{BC}
$I_{\overline{CE}}$	Chip enable input current	-	-	100	µA	Internal 50K pull-up

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V

Notes: Typical values indicate operation at T_A = 25°C.
Potentials are relative to V_{SS}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested.

4

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 5 and 6

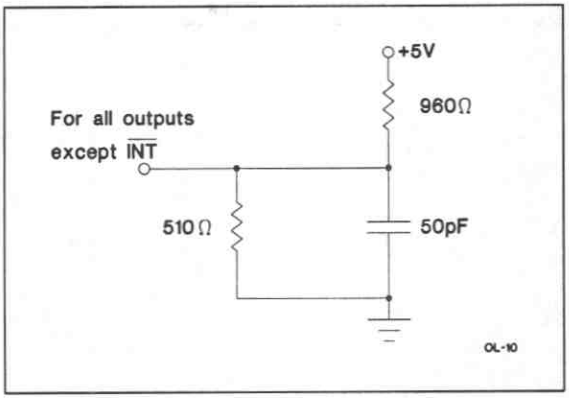


Figure 5. Output Load A

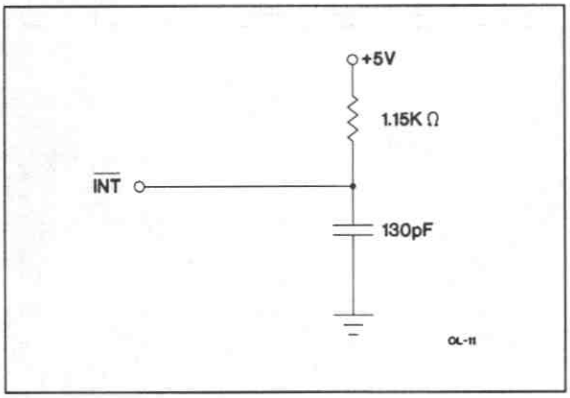
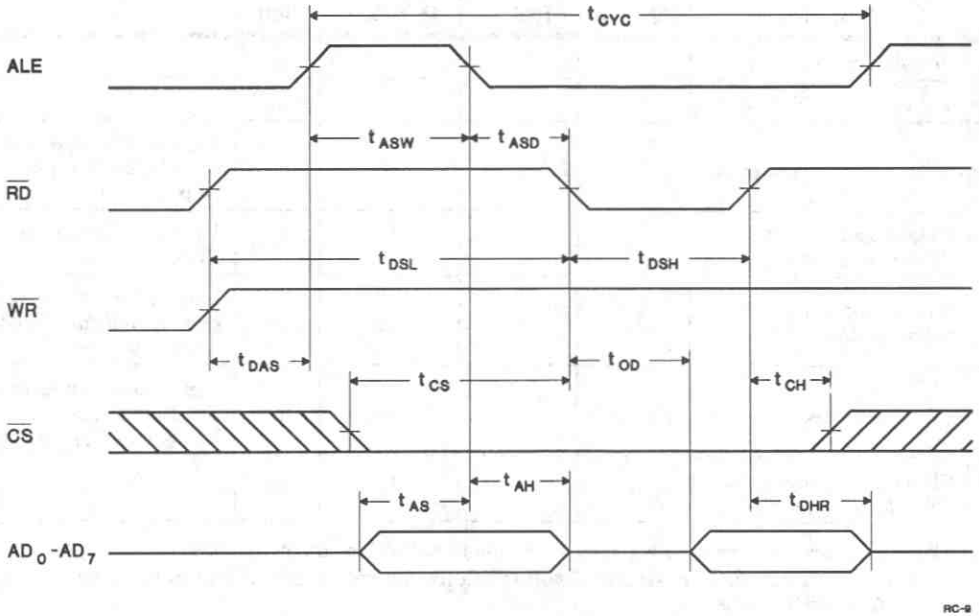


Figure 6. Output Load B

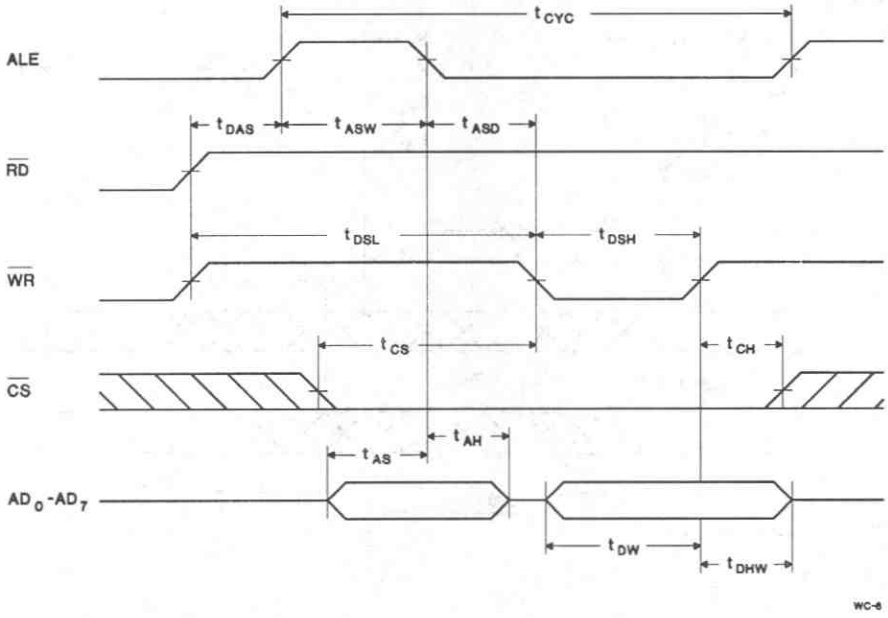
Read/Write Timing (TA = TOPR, VCC = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160	-	-	ns	
t_{DSL}	$\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	$\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{RWH}	$\overline{WR}$ hold time	0	-	-	ns	
t_{RWS}	$\overline{WR}$ setup time	10	-	-	ns	
t_{CS}	Chip select setup time	5	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{DAS}	Delay time, $\overline{RD}$ to ALE rise	10	-	-	ns	
t_{ASW}	Pulse width, ALE high	30	-	-	ns	
t_{ASD}	Delay time, ALE to $\overline{RD}/\overline{WR}$ fall	35	-	-	ns	
t_{OD}	Output data delay time from $\overline{RD}$ fall	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 2
t_{UC}	Time of update cycle	-	1	-	µs	

Read Timing



Write Timing



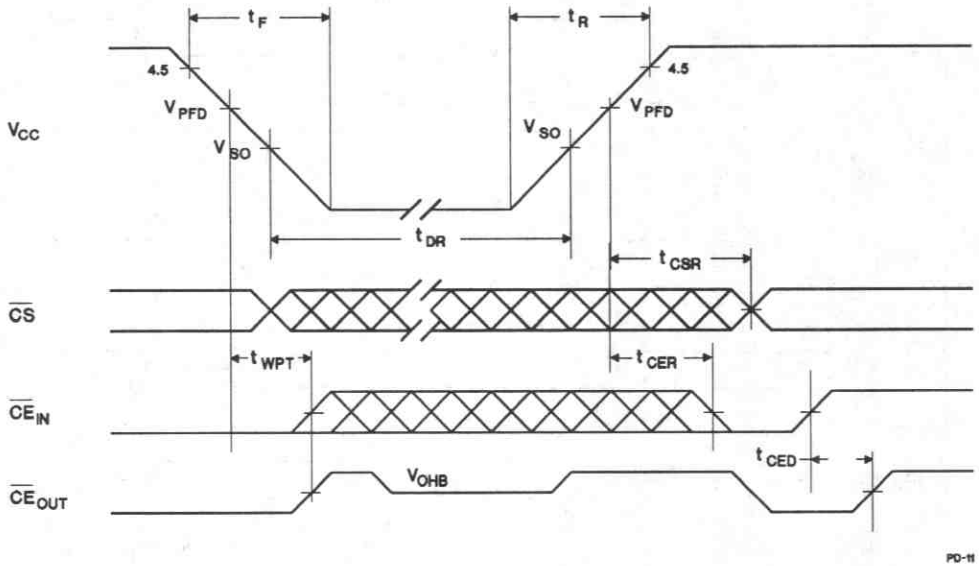
Power-Down/Power-Up Timing (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention and timekeeping time	10	-	-	years	T_A = 25°C, no load on V_{OUT} or $\overline{CE}_{OUT}$.
t_{WPT}	Write-protect time for external RAM	10	16	30	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.
t_{CER}	Chip enable recovery time	t_{CSR}	-	t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM	-	7	10	ns	

Note: Clock accuracy is better than ± 1 minute per month at 25°C for the period of t_{DR}.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

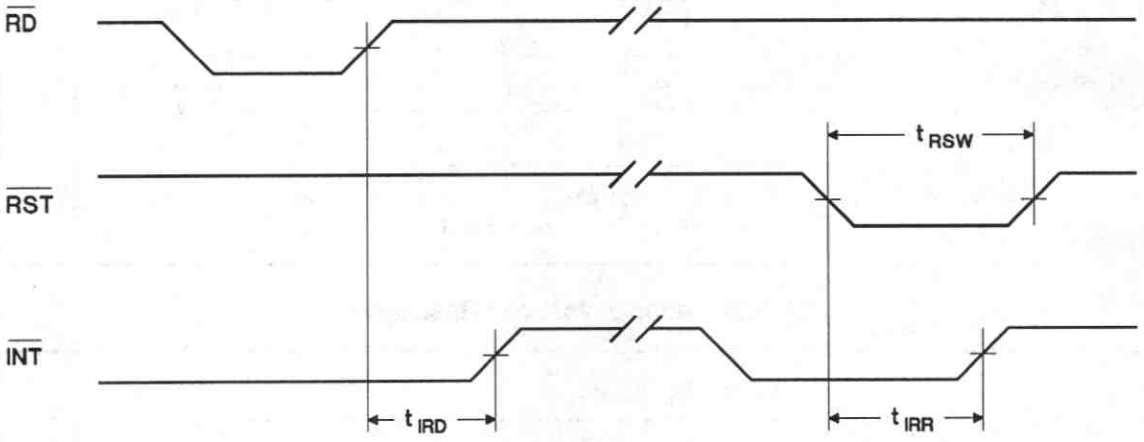
Power-Down/Power-Up Timing



Interrupt Delay Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from $\overline{RD}$	-	-	2	µs

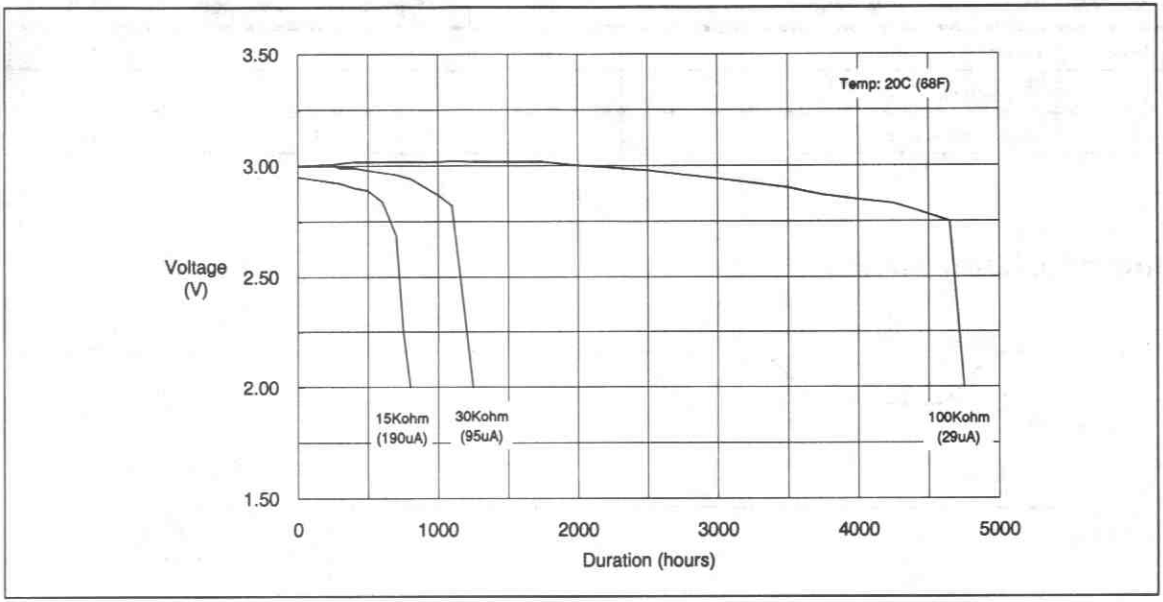
Interrupt Delay Timing



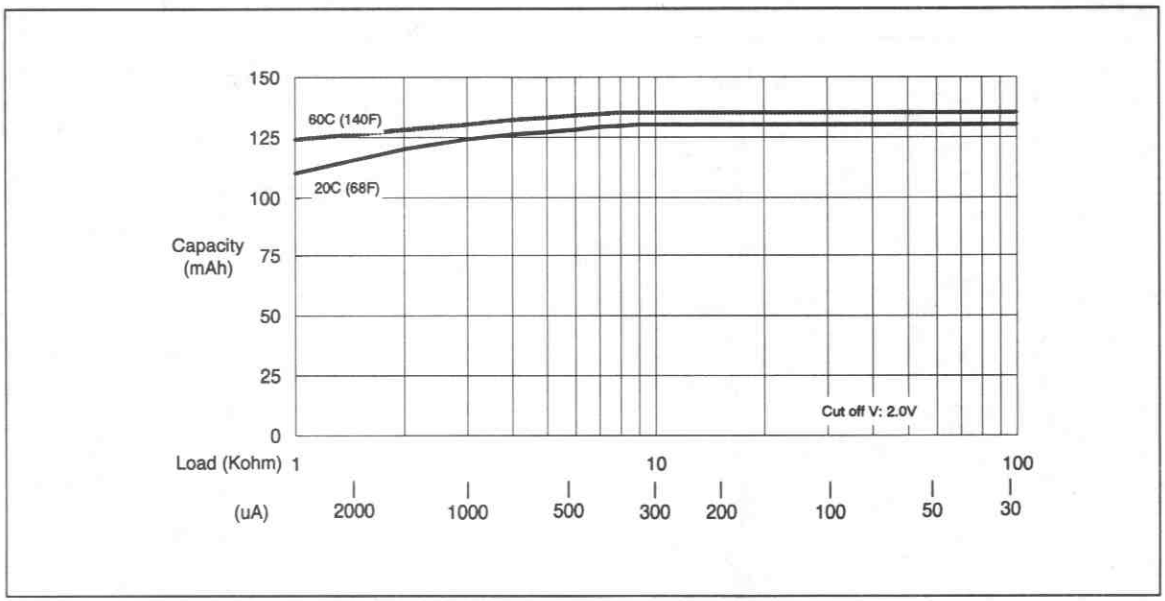
INT-3

Typical Battery Characteristics (source = Panasonic)

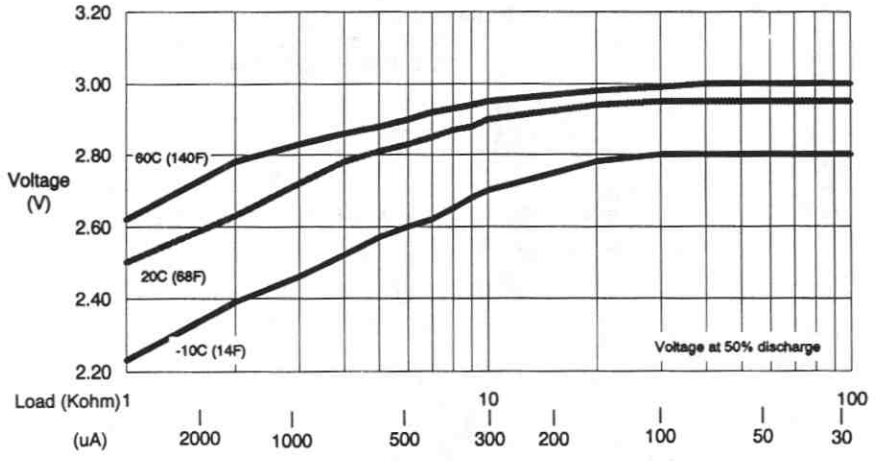
CR1632 Load Characteristics



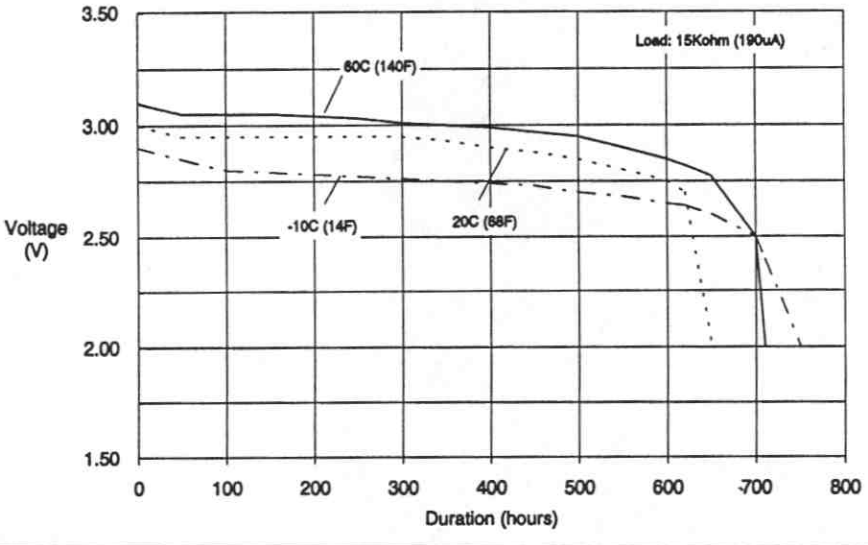
CR1632 Capacity vs. Load Resistance



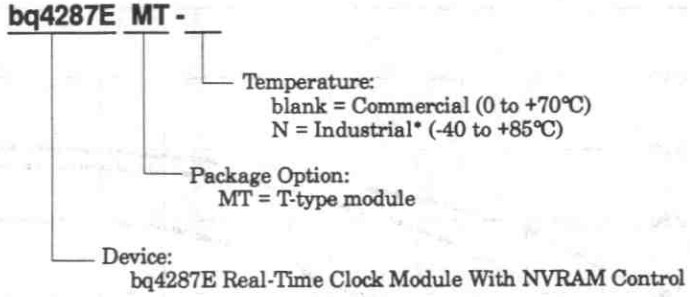
CR1632 Operating Voltage vs. Load Resistance



CR1632 Temperature Characteristics



Ordering Information



*Contact factory for availability.

BENCHMARQ

Preliminary bq4016/bq4016Y

1024Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Conventional SRAM operation; unlimited write cycles
- 10-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4016 is a nonvolatile 8,388,608-bit static RAM organized as 1,048,576 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

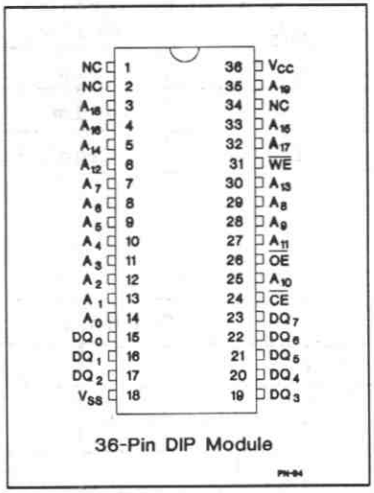
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4016 uses extremely low standby current CMOS SRAMs, coupled with a small lithium coin cell to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4016 has the same interface as industry-standard SRAMs and requires no external circuitry.

Pin Connections



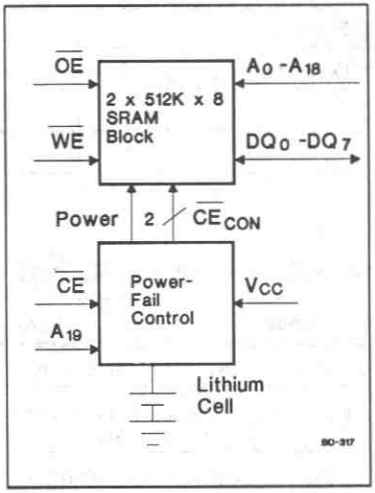
36-Pin DIP Module

PN-04

Pin Names

A_0–A_{19}	Address inputs
DQ_0–DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground
NC	No connect

Block Diagram



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Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4016MC -70	70	-5%	bq4016YMC -70	70	-10%

Functional Description

When power is valid, the bq4016 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4016 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4016 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4016Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4016 have an extremely long shelf life. The bq4016 provides data retention for more than 10 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4016Y
		4.75	5.0	5.5	V	bq4016
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 2	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 2	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	5	12	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	5	mA	$0V \leq V_{IN} \leq 0.2V$, $\overline{CE} \geq V_{CC}$ - 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2
I_{CC}	Operating supply current	-	75	115	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA, A19 < V_{IL} or A19 > V_{IH},
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4016
		4.30	4.37	4.50	V	bq4016Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

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Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	20	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	20	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

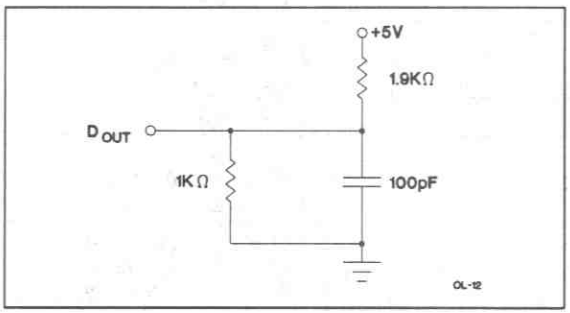


Figure 1. Output Load A

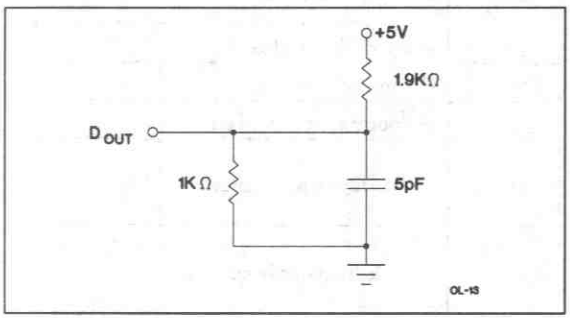
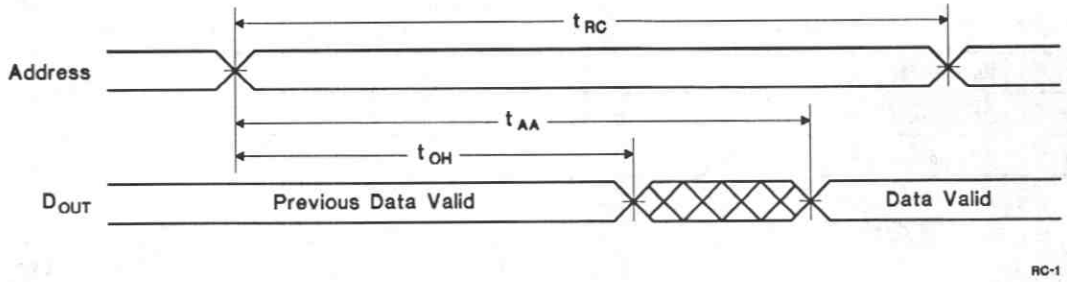


Figure 2. Output Load B

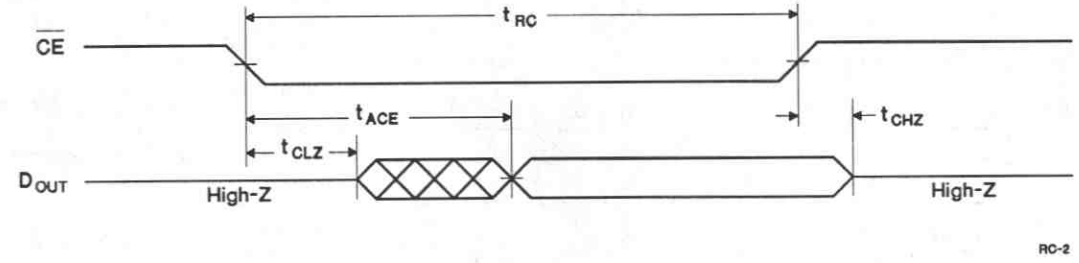
Read Cycle (T_A = 0 to 70°C, $V_{CC}min \le V_{CC} \le V_{CC}max$)

Symbol	Parameter	-70		Unit	Conditions
		Min.	Max.		
t_{RC}	Read cycle time	70	-	ns	
t_{AA}	Address access time	-	70	ns	Output load A
t_{ACE}	Chip enable access time	-	70	ns	Output load A
t_{OE}	Output enable to output valid	-	35	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10	-	ns	Output load A

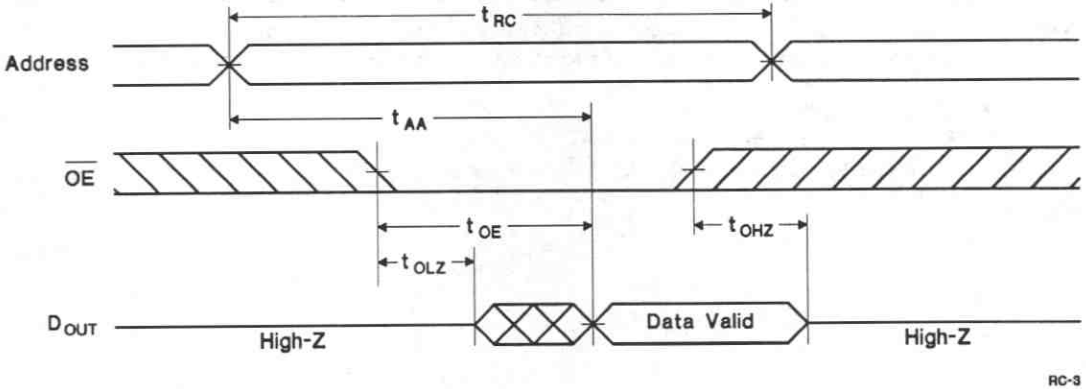
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

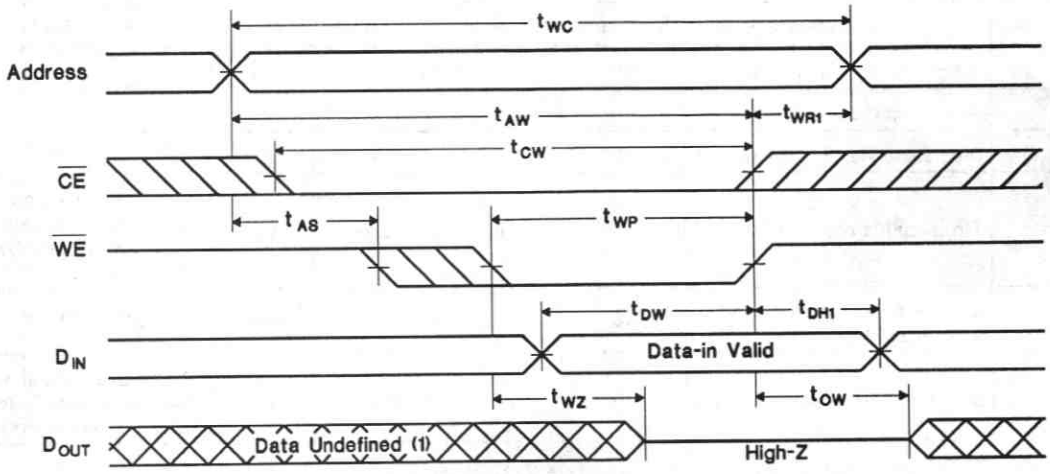
Write Cycle (T_A = 0 to 70°C, $V_{CC}min \le V_{CC} \le V_{CC}max$)

Symbol	Parameter	-70		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	70	-	ns	
t_{CW}	Chip enable to end of write	65	-	ns	(1)
t_{AW}	Address valid to end of write	65	-	ns	(1)
t_{AS}	Address setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	ns	I/O pins are in output state. (5)

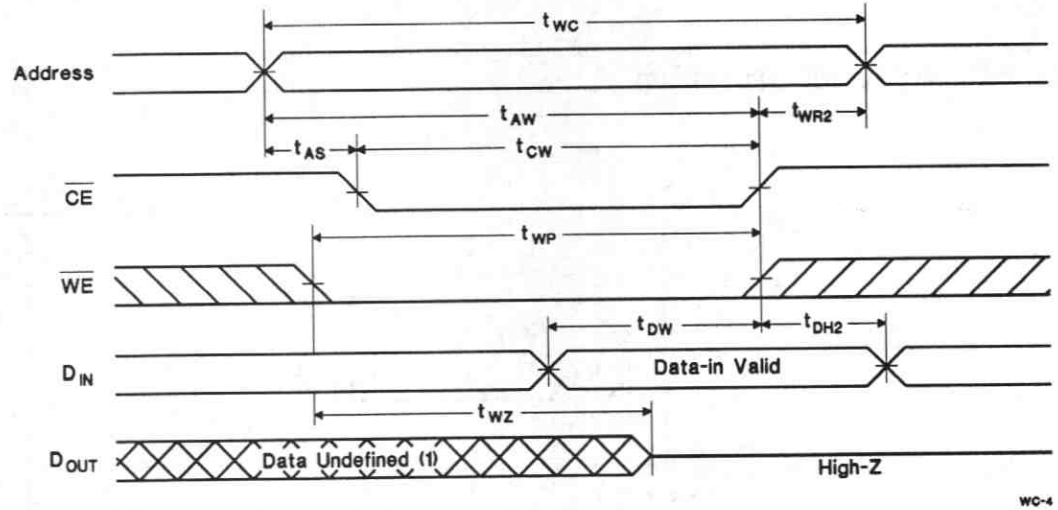
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

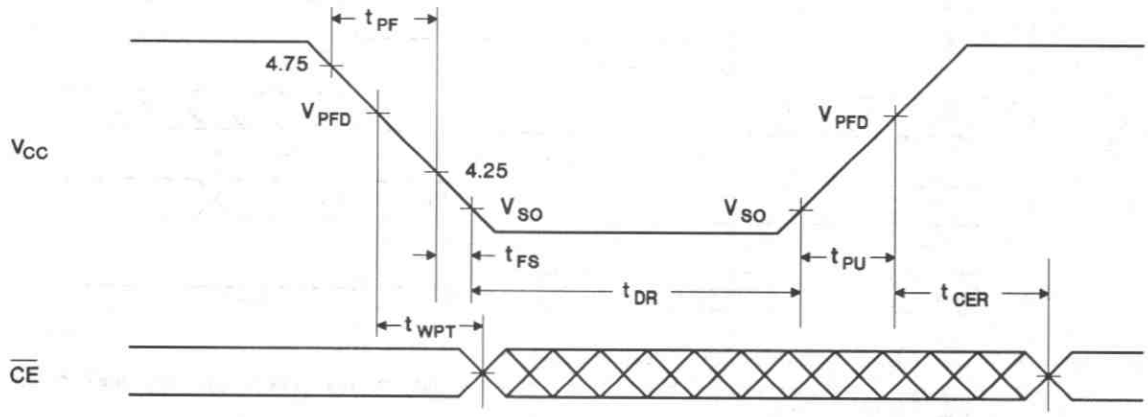
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{FPD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	10	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

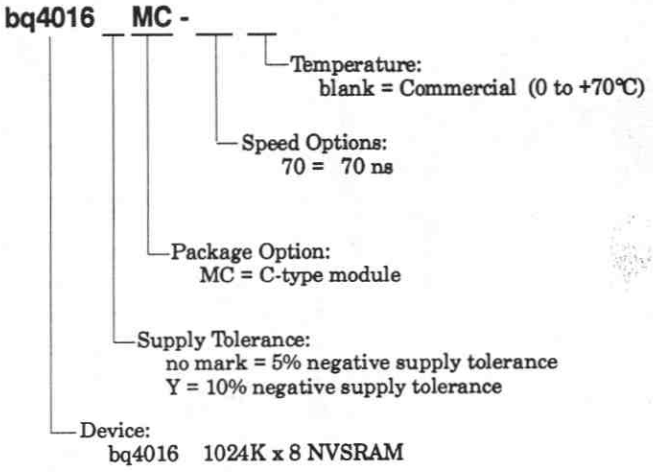
Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-B

Ordering Information



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Notes

BENCHMARQ

Preliminary bq4017/bq4017Y

2048Kx8 Nonvolatile SRAM

Features

- Data retention in the absence of power
- Automatic write-protection during power-up/power-down cycles
- Conventional SRAM operation; unlimited write cycles
- 5-year minimum data retention in absence of power
- Battery internally isolated until power is applied

General Description

The CMOS bq4017 is a nonvolatile 16,777,216-bit static RAM organized as 2,097,152 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

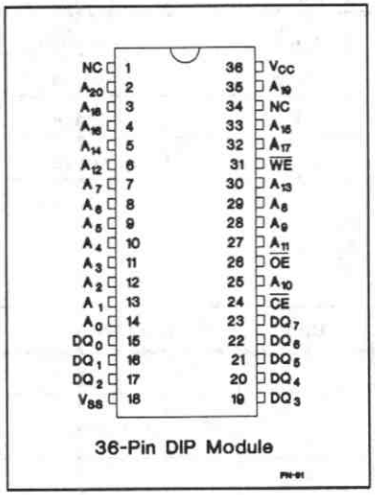
The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write operation.

At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The bq4017 uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4017 has the same interface as industry-standard SRAMs and requires no external circuitry.

Pin Connections

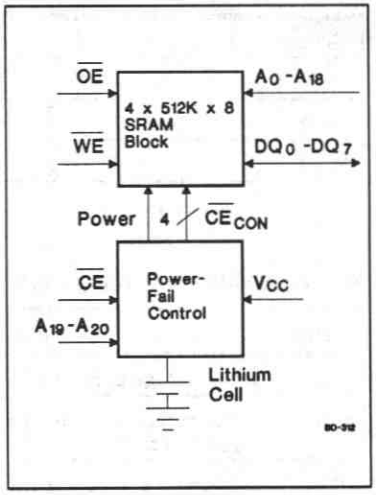


36-Pin DIP Module

Pin Names

A_0–A_{20}	Address inputs
DQ_0–DQ_7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
V_{CC}	+5 volt supply input
V_{SS}	Ground
NC	No connect

Block Diagram



Selection Guide

Part Number	Maximum Access Time (ns)	Negative Supply Tolerance	Part Number	Maximum Access Time (ns)	Negative Supply Tolerance
bq4017MC -70	70	-5%	bq4017YMC -70	70	-10%

Functional Description

When power is valid, the bq4017 operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4017 acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4017 monitors for V_{PFD} = 4.62V typical for use in systems with 5% supply tolerance. The bq4017Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4017 have an extremely long shelf life. The bq4017 provides data retention for more than 5 years in the absence of system power.

As shipped from Benchmarq, the integral lithium cells are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	Power
Not selected	H	X	X	High Z	Standby
Output disable	L	H	H	High Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-40 to +70	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4017Y
		4.75	5.0	5.5	V	bq4017
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 4	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 4	µA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.1 mA
I_{SB1}	Standby supply current	-	7	17	mA	$\overline{CE} = V_{IH}$
I_{SB2}	Standby supply current	-	2.5	5	mA	$0V \leq V_{IN} \leq 0.2V$, $\overline{CE} \geq V_{CC}$ - 0.2V, or $V_{IN} \geq V_{CC}$ - 0.2
I_{CC}	Operating supply current	-	75	115	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$, $I_{I/O}$ = 0mA, A19 < V_{IL} or A19 > V_{IH}, A20 < V_{IL} or A20 > V_{IH}
V_{PFD}	Power-fail-detect voltage	4.55	4.62	4.75	V	bq4017
		4.30	4.37	4.50	V	bq4017Y
V_{SO}	Supply switch-over voltage	-	3	-	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

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Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	40	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	40	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

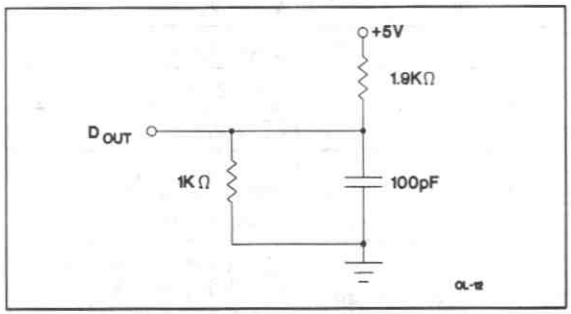


Figure 1. Output Load A

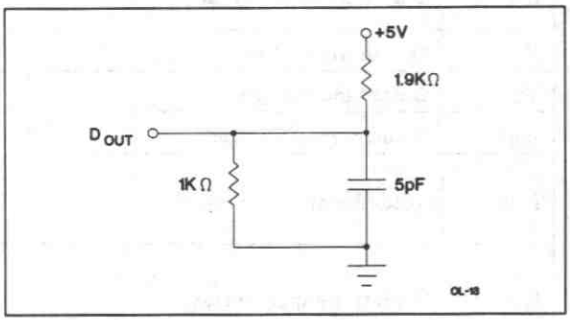
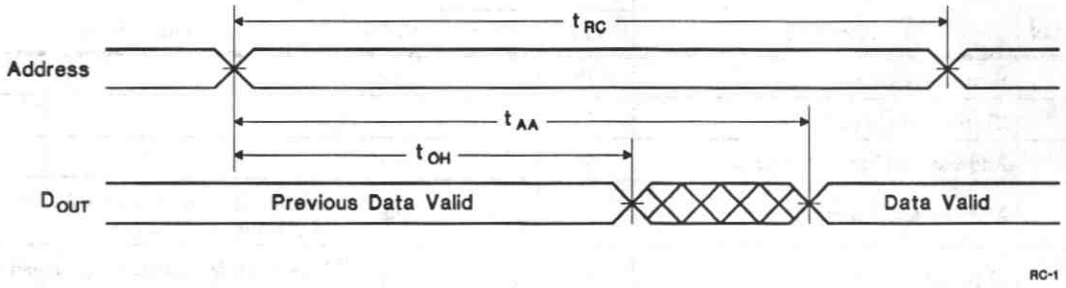


Figure 2. Output Load B

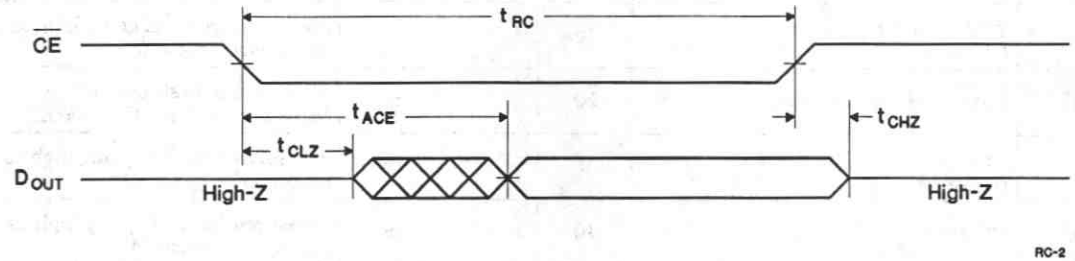
Read Cycle (T_A = 0 to 70°C, $V_{CCmin} \le V_{CC} \le V_{CCmax}$)

Symbol	Parameter	-70		Unit	Conditions
		Min.	Max.		
t_{RC}	Read cycle time	70	-	ns	
t_{AA}	Address access time	-	70	ns	Output load A
t_{ACE}	Chip enable access time	-	70	ns	Output load A
t_{OE}	Output enable to output valid	-	35	ns	Output load A
t_{CLZ}	Chip enable to output in low Z	5	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	5	-	ns	Output load B
t_{CHZ}	Chip disable to output in high Z	0	25	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	25	ns	Output load B
t_{OH}	Output hold from address change	10	-	ns	Output load A

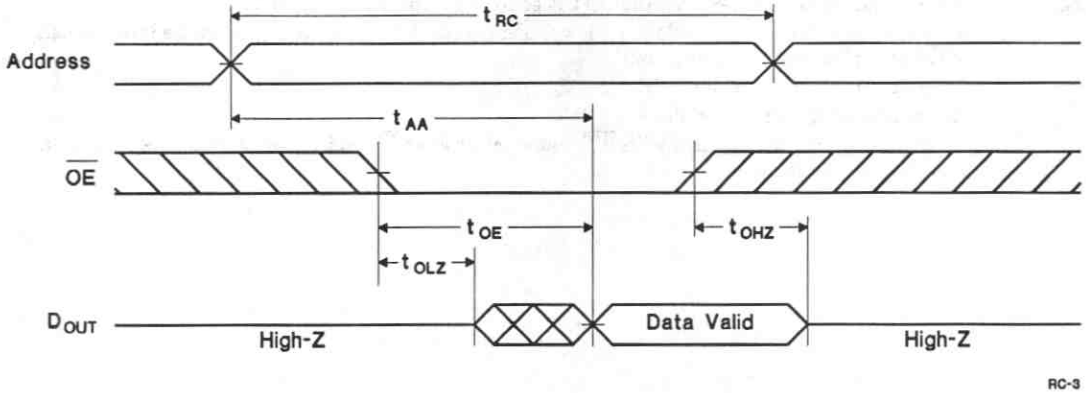
Read Cycle No. 1 (Address Access) [1,2]



Read Cycle No. 2 ($\overline{CE}$ Access) [1,3,4]



Read Cycle No. 3 ($\overline{OE}$ Access) [1,5]



Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CE} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CE} = V_{IL}$.

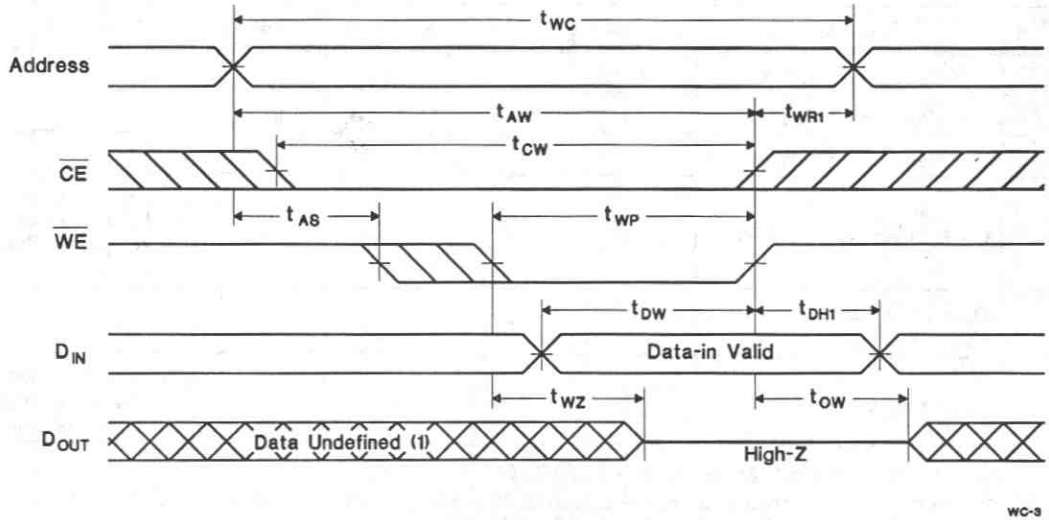
Write Cycle (T_A = 0 to 70°C, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	-70		Units	Conditions/Notes
		Min.	Max.		
t_{WC}	Write cycle time	70	-	ns	
t_{CW}	Chip enable to end of write	65	-	ns	(1)
t_{AW}	Address valid to end of write	65	-	ns	(1)
t_{AS}	Address setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	55	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	30	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	25	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	5	-	ns	I/O pins are in output state. (5)

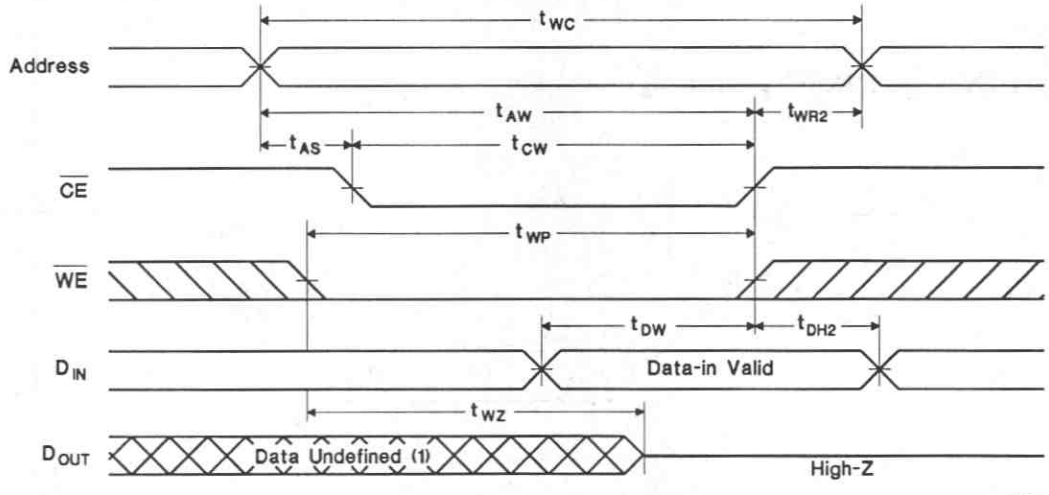
Notes:

1. A write ends at the earlier transition of $\overline{CE}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CE}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Write Cycle No. 1 ($\overline{WE}$-Controlled) [1,2,3]



Write Cycle No. 2 ($\overline{CE}$-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
2. Because I/O may be active ($\overline{OE}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

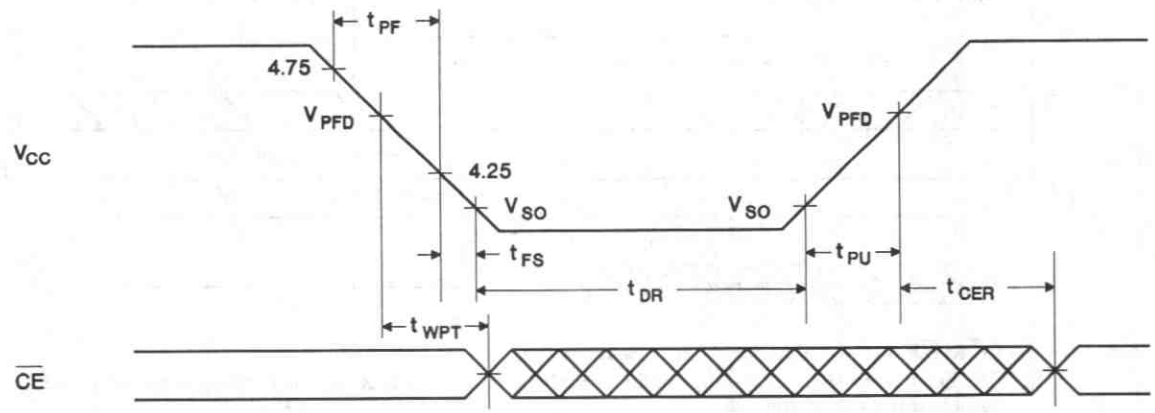
Power-Down/Power-Up Cycle (T_A = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	0	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	5	-	-	years	T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.

Note: 1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

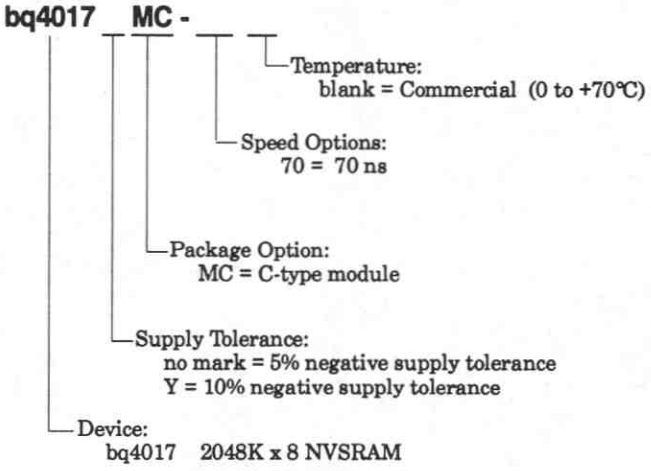
Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

Power-Down/Power-Up Timing



PD-B

Ordering Information



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Notes

BENCHMARQ

Package Drawings

Benchmarq's standard packages are described in the following tables.

Package Type	Description	No. Pins	Device
MA	DIP Module, A-Type	12	bq2502
		28	bq4010/bq4010Y
			bq4011Y/bq4011Y
			bq4830Y
		32	bq4013/bq4013Y
			bq4015/bq4015Y
			bq4832Y
			bq4842Y
		40	bq4024/bq4024Y
			bq4025/bq4025Y
			bq4115Y
MB	DIP Module, B-Type	32	bq4014/bq4014Y
			bq4015/bq4015Y
MC	DIP Module, C-Type	36	bq4016/4016Y
			bq4017/4017Y
MT	DIP Module, T-Type	24	bq3287/bq3287A
			bq3287E/bq3287EA
			bq4287/bq4287E
		28	bq4847/bq4847Y
P	Plastic DIP, 0.600"	24	bq3285
			bq3285E
			bq3285L
			bq4285
			bq4285E
			bq4285L
		28	bq4845/bq4845Y

Package Type	Description	No. Pins	Device
PN	Plastic DIP, 0.300"	8	bq2002
			bq2002T
			bq2201
			bq2053
			bq2902
		14	bq2903
		16	bq2003
			bq2004
			bq2004E
			bq2010
			bq2011
			bq2012
			bq2014
			bq2031
			bq2040
			bq2050
			bq2054
			bq2202
			bq2203A
			bq2204A
			bq2212
		20	bq2005
		24	bq2001
			bq2007

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Package Drawings

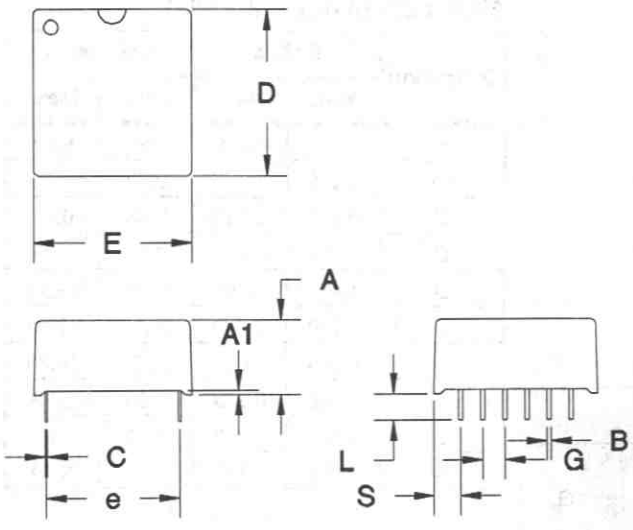
Package Type	Description	No. Pins	Device
Q	Quad PLCC	28	bq3285
			bq3285E
			bq4285
			bq4285E
S	SOIC, 0.300"	16	bq2003
		20	bq2005
		24	bq2001
			bq2007
			bq3285
			bq3285E
			bq3285L
			bq4285
			bq4285E
			bq4285L
		28	bq4845/Y

* Contact factory for availability.

Package Type	Description	No. Pins	Device
SN	SOIC Narrow, 0.150"	8	bq2002
			bq2201
			bq2053
			bq2902
		14	bq2903
		16	bq2004
			bq2004E
			bq2010
			bq2011
			bq2012
			bq2014
			bq2031
			bq2040
			bq2050
			bq2054
			bq2202
			bq2203A
			bq2204A
			bq2212
SS*	SSOP, 0.150"	24	bq3285E
			bq3285L
			bq4285E
			bq4285L

* Contact factory for availability.

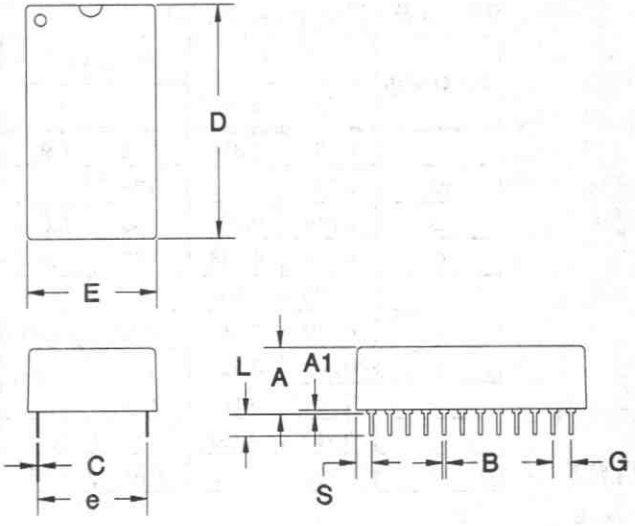
MA: 12-Pin A-Type Module



12-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	8.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	0.710	0.740	18.03	18.80
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.105	0.130	2.67	3.30

MT: 24-Pin T-Type Module

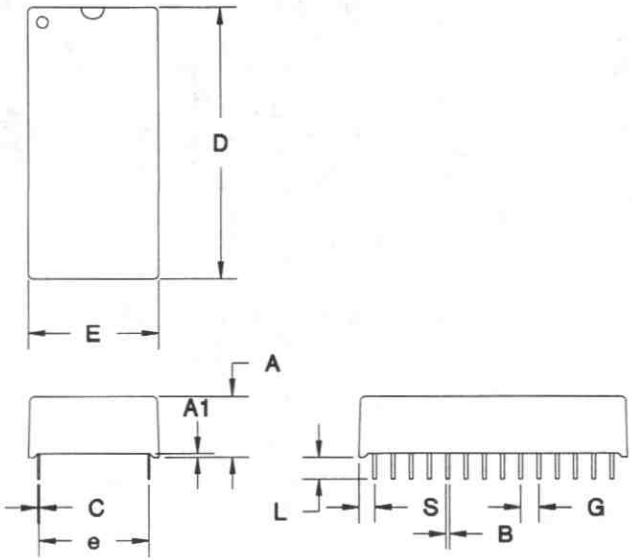


24-Pin MT (T-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.360	0.390	9.14	9.91
A1	0.015	-	0.38	-
B	0.015	0.022	0.38	0.56
C	0.008	0.013	0.20	0.33
D	1.320	1.335	33.53	33.91
E	0.710	0.740	18.03	18.80
e	0.590	0.620	14.99	15.75
G	0.090	0.110	2.29	2.79
L	0.110	0.130	2.79	3.30
S	0.100	0.120	2.54	3.05

Package Drawings

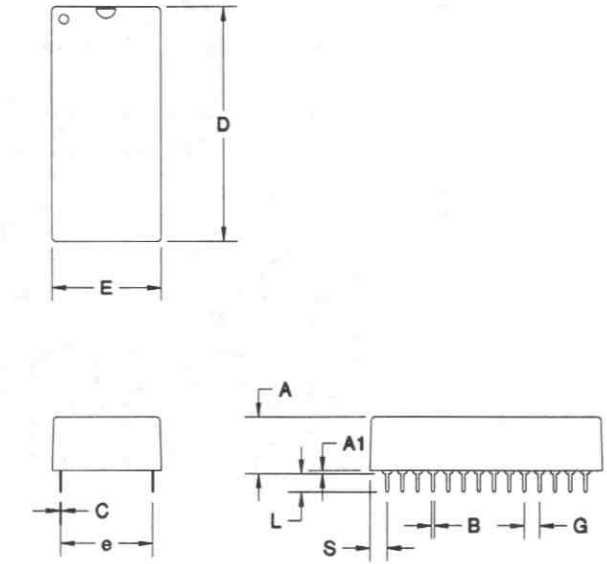
MA: 28-Pin A-Type Module



28-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	1.470	1.500	37.34	38.10
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

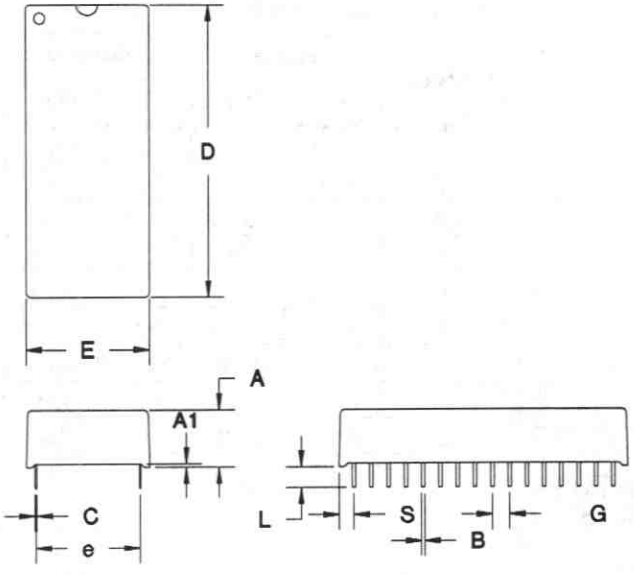
MT: 28-Pin T-Type Module



28-Pin MT (T-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.360	0.390	9.14	9.91
A1	0.015	-	0.38	-
B	0.015	0.022	0.38	0.56
C	0.008	0.013	0.20	0.33
D	1.520	1.535	38.61	38.99
E	0.710	0.740	18.03	18.80
e	0.590	0.620	14.99	15.75
G	0.090	0.110	2.29	2.79
L	0.110	0.130	2.79	3.30
S	0.100	0.120	2.54	3.05

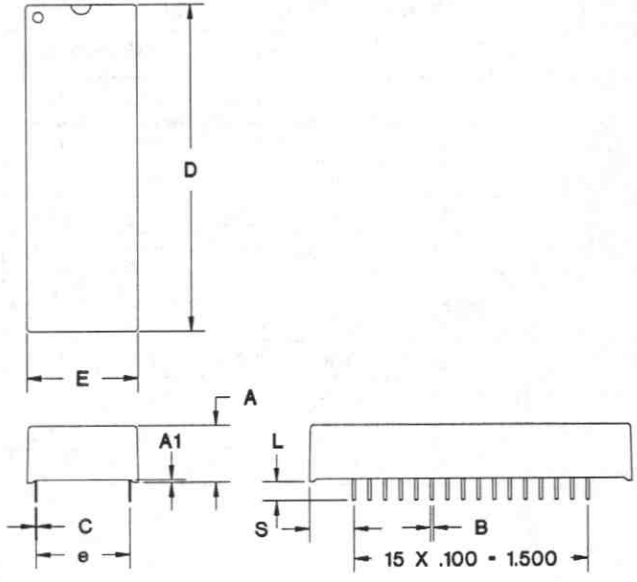
MA: 32-Pin A-Type Module



32-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	1.670	1.700	42.42	43.18
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

MB: 32-Pin B-Type Module

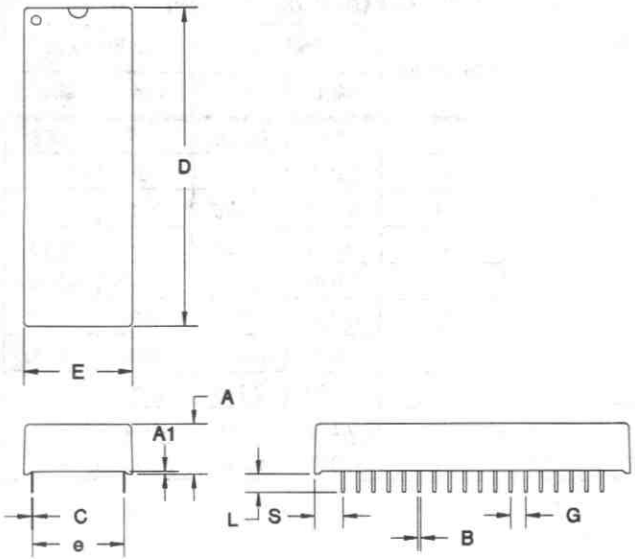


32-Pin MB (B-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	2.070	2.100	52.58	53.34
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.275	0.310	6.99	7.87

Package Drawings

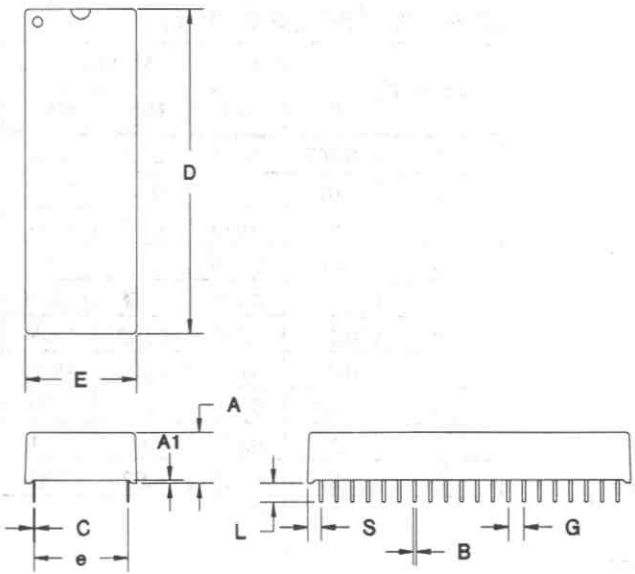
MC: 36-Pin C-Type Module



36-Pin MC (C-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	2.070	2.100	52.58	53.34
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.175	0.210	4.45	5.33

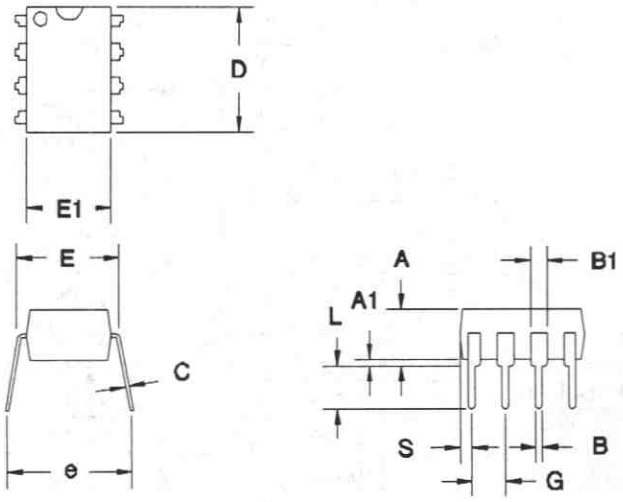
MA: 40-Pin A-Type Module



40-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	2.070	2.100	52.58	53.34
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

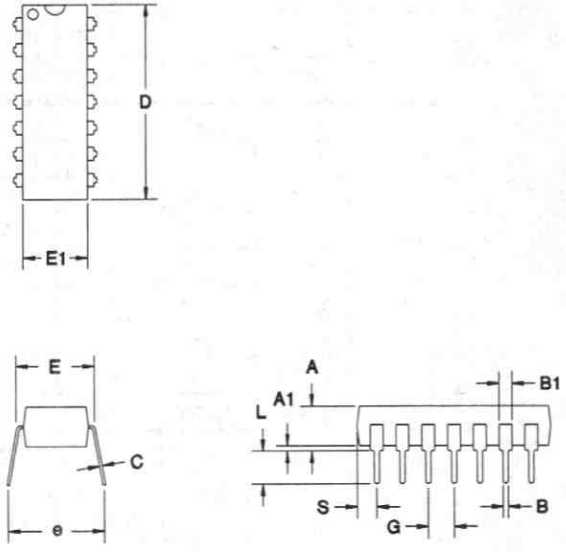
PN: 8-Pin DIP (0.300")



8-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.350	0.380	8.89	9.65
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

PN: 14-Pin DIP (0.300")

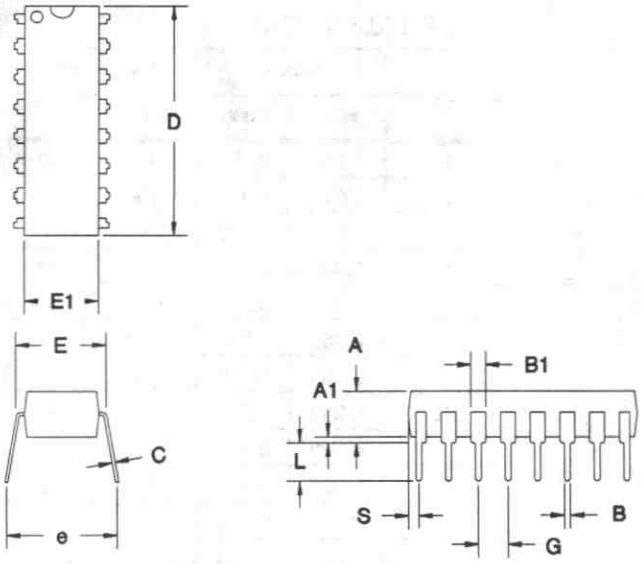


14-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

Package Drawings

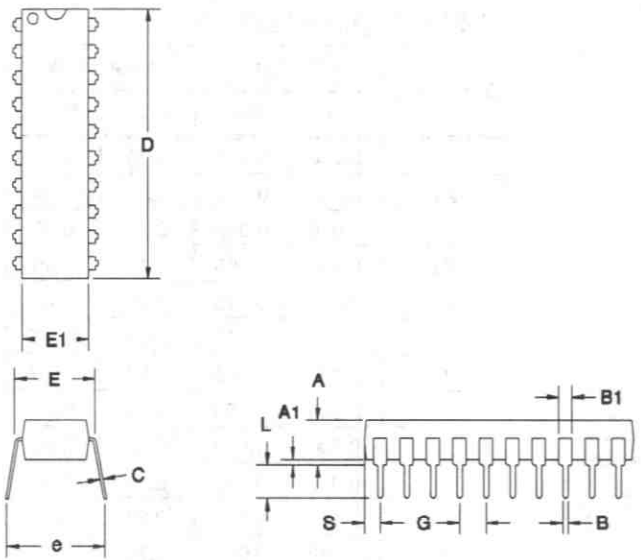
PN: 16-Pin DIP (0.300")



16-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

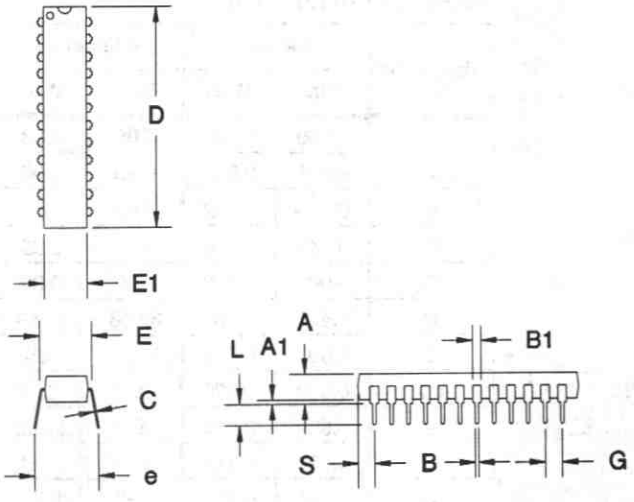
PN: 20-Pin DIP (0.300")



20-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	1.010	1.060	25.65	26.92
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.135	2.92	3.43
S	0.055	0.080	1.40	2.03

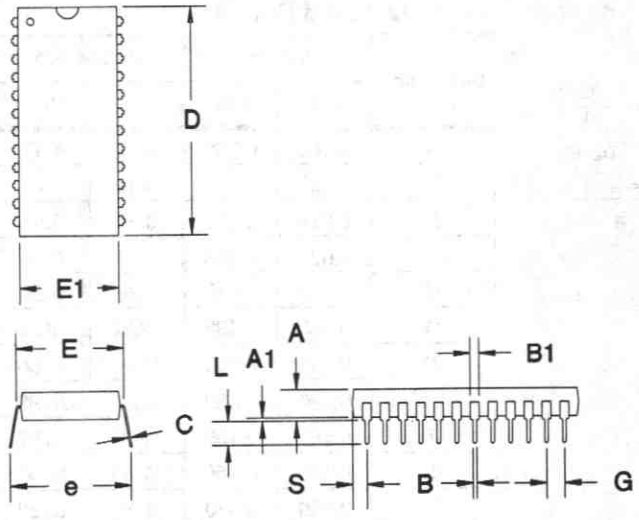
PN: 24-Pin DIP (0.300")



24-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.055	1.14	1.40
C	0.008	0.013	0.20	0.33
D	1.240	1.280	31.50	32.51
E	0.300	0.325	7.62	8.26
E1	0.250	0.300	6.35	7.62
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

P: 24-Pin DIP (0.600")

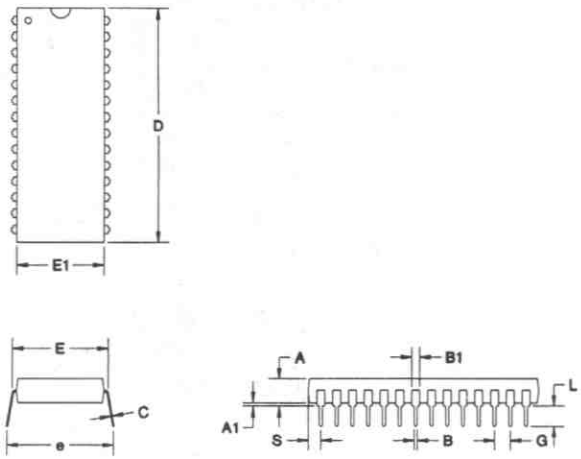


24-Pin DIP (0.600" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.190	4.06	4.83
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.013	0.20	0.33
D	1.240	1.280	31.50	32.51
E	0.600	0.625	15.24	15.88
E1	0.530	0.570	13.46	14.48
e	0.600	0.670	15.24	17.02
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

Package Drawings

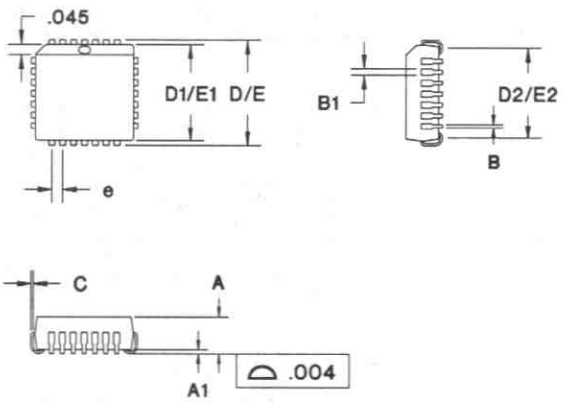
P: 28-Pin DIP (0.600")



28-Pin DIP (0.600" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.190	4.06	4.83
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.013	0.20	0.33
D	1.440	1.480	36.58	37.59
E	0.600	0.625	15.24	15.88
E1	0.530	0.570	13.46	14.48
e	0.600	0.670	15.24	17.02
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

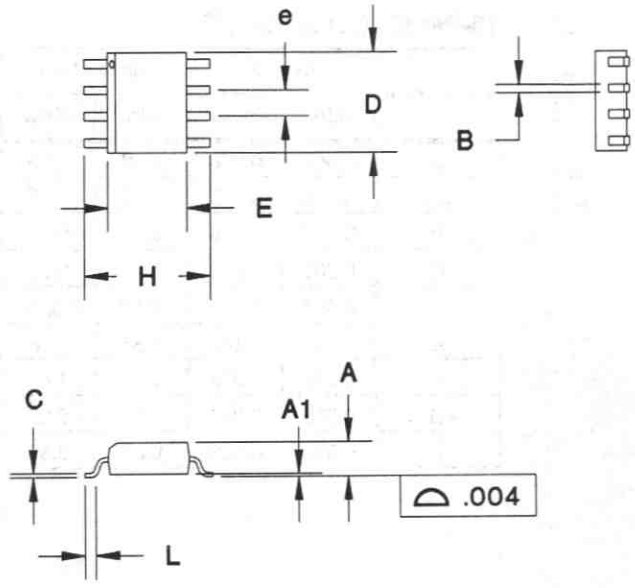
Q: 28-Pin Quad PLCC



28-Pin Q (Quad PLCC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.165	0.180	4.19	4.57
A1	0.020	-	0.51	-
B	0.012	0.021	0.30	0.53
B1	0.025	0.033	0.64	0.84
C	0.008	0.012	0.20	0.30
D	0.485	0.495	12.32	12.57
D1	0.445	0.455	11.30	11.56
D2	0.390	0.430	9.91	10.92
E	0.485	0.495	12.32	12.57
E1	0.445	0.455	11.30	11.56
E2	0.390	0.430	9.91	10.92
e	0.045	0.055	1.14	1.40

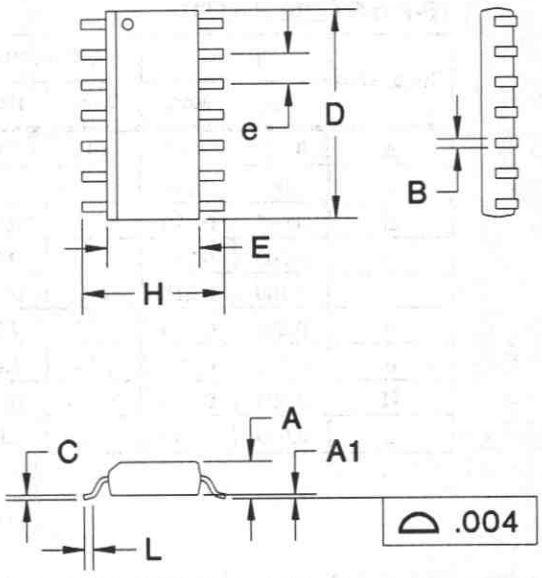
SN: 8-Pin SN (0.150" SOIC)



8-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.185	0.200	4.70	5.08
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

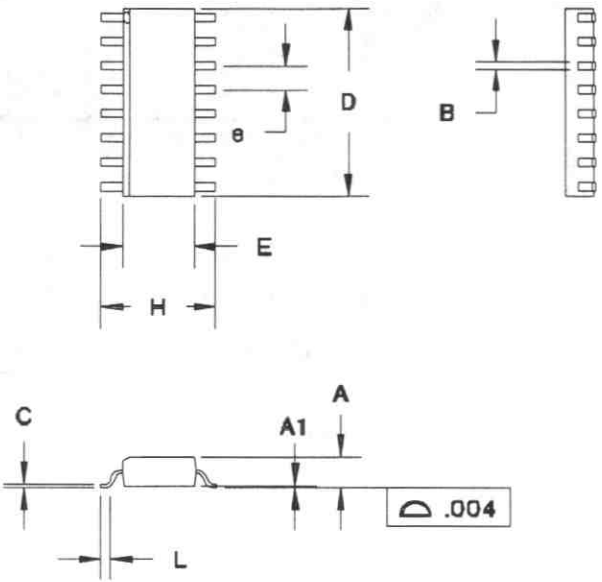
SN: 14-Pin SN (0.150" SOIC)



14-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.335	0.350	8.51	8.89
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

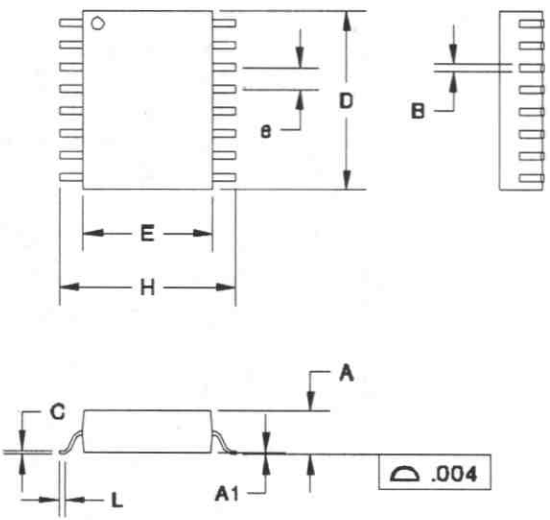
SN: 16-Pin SN (0.150" SOIC)



16-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

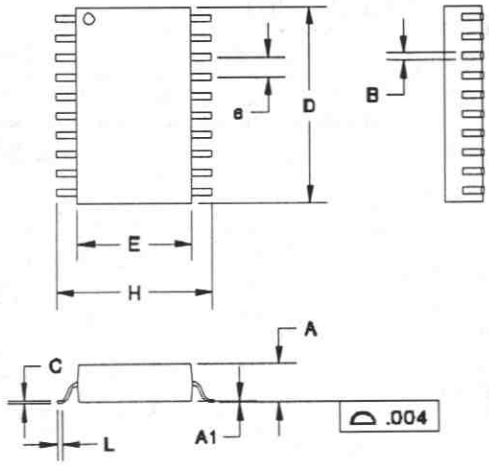
S: 16-Pin S (0.300" SOIC)



16-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.400	0.415	10.16	10.54
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

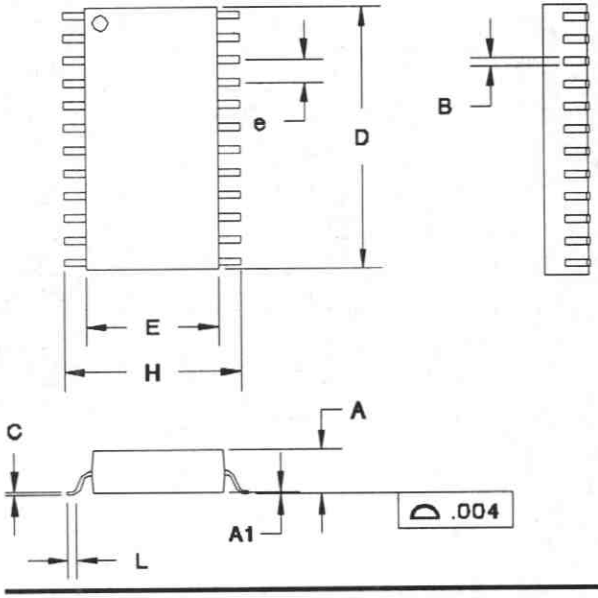
S: 20-Pin S (0.300" SOIC)



20-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.500	0.515	12.70	13.08
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

S: 24-Pin S (0.300" SOIC)

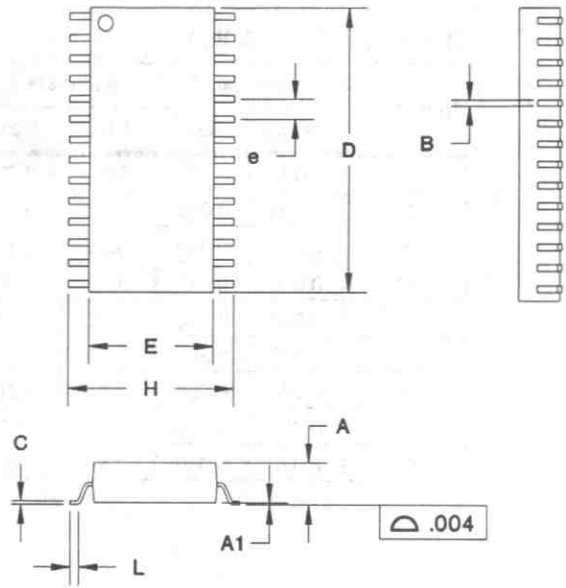


24-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.600	0.615	15.24	15.62
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

Package Drawings

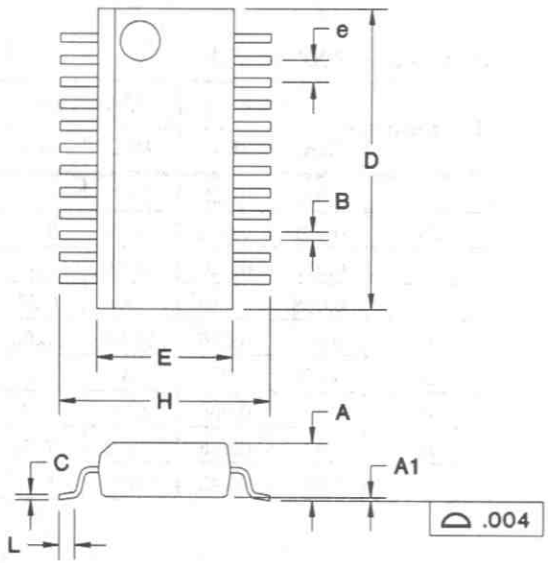
S: 28-Pin S (0.300" SOIC)



28-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.700	0.715	17.78	18.16
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

24-Pin SSOP (SS)



24-Pin SS (0.150" SSOP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.061	0.068	1.55	1.73
A1	0.004	0.010	0.10	0.25
B	0.008	0.012	0.20	0.30
C	0.007	0.010	0.18	0.25
D	0.337	0.344	8.56	8.74
E	0.150	0.157	3.81	3.99
e	.025 BSC		0.64 BSC	
H	0.230	0.244	5.84	6.20
L	0.016	0.035	0.41	0.89

The Benchmarq Quality Policy

It is the policy of Benchmarq to provide the highest-quality products in support of our customers' needs. We recognize that we are in the business of providing not only the physical product, but also documentation, technical support, sales and marketing support, and timely product delivery. Our commitment to our customers begins with product concept and must extend long after actual product purchase and receipt.

We are dedicated to establishing partnerships with our customers and know that to succeed we must help our customers succeed. We will do this by:

- Holding ourselves and our vendors accountable for establishing carefully considered methods and procedures for design, test, and production with clear and concise documentation,
- Responding professionally and expeditiously to customer or vendor problems that arise, bringing to bear the company's strongest resources,
- Developing an industry-leading "Quality Technology" to drive incremental improvements in all the products we provide, and to contribute to a continuous reduction in new product time to market, and
- Continuously providing products and services that meet or exceed the best expectations of our customers.

In pursuing this commitment to quality, we have performed extensive qualification testing on our devices to help ensure the highest levels of product reliability.

We feel confident that the reliability levels demonstrated by our qualification testing will allow us to provide a high-quality product that will meet or exceed our customers' needs. Benchmarq is continuously working toward improving product reliability.

An integral part of quality improvement is customer feedback. We encourage our customers to contact us with any questions or suggestions regarding their individual quality requirements or for information concerning up-to-date product enhancements.

Call us—we want to hear from you.

Underwriters Laboratory Recognition

Benchmarq's ICs and modules have been recognized by Underwriters Laboratory (U.L.®) under file E134016 (R). This helps to hasten U.L. approval of our customers' end equipment.

*For detailed *Quality and Reliability Reports*, contact the factory or your sales representative.

Quality Procedures

To help ensure that our final product is both consistent and reliable, the following quality tests and procedures have been implemented.

Test Probe

Each wafer is electrically tested at test probe to verify parametric integrity. Any wafer not meeting parametric specifications is rejected.

Wafer IQC

Wafer samples are periodically subjected to physical cross-sectional analysis to verify conformance to design and process specifications.

Final Visual

All lots are subjected to QC final visual inspection. The travelers are checked to make sure that the product was properly burned-in and tested. Additionally, lot numbers and counts are verified, and the devices are checked for mechanical integrity.

Board-Level Products

All printed circuit board level products are manufactured to meet ANSI/IPC-A-610A and ANSI/IPC-A-600D Class 2 specifications.

Traceability

Full traceability is maintained on all products. The devices are traceable to front-end wafer lot and to assembly lot. Top brand includes the Benchmarq logo, part number, date code, and unique lot number (module products).

Electrostatic Discharge (ESD)

It is recognized that electronic components are susceptible to damage due to electrostatic discharge. To help minimize this risk, the following safeguards have been put into place:

- All personnel who handle devices wear grounded wrist and heel straps and have been trained to use proper device-handling procedures.
- All work surfaces used in the test and QC areas have been grounded. Antistatic flooring is used in the test, QC, and finished goods areas.
- All device testers and handlers have adequate grounding.
- Devices are placed into antistatic tubes and kept in conductive totes or boxes during the manufacturing process.
- Finished goods are stored in conductive boxes. Boxes and shipping containers are labeled with ESD warnings.

Packing and Shipping

Great care is taken to ensure that finished product reaches the customer in perfect condition. All devices are placed in antistatic tubes during the assembly and test operations. Before shipping, device tubes are placed in conductive boxes that are marked with ESD warning labels. The conductive boxes are then placed into non-conductive shipping containers for additional protection against rough handling. The shipping containers are also marked with ESD caution labels.

Process Monitoring

The materials, assembly process, and test process are constantly monitored for problems and inconsistencies. Operator traceability and accountability are maintained so that any problems can be identified earlier and corrections implemented quicker. The wafer foundry and assembly contractor are required to use Statistical Process Control (SPC) techniques to demonstrate that their manufacturing processes and hence, their final products, are in control and will not vary from lot to lot. This constant effort is provided to ensure the highest possible product quality.

Qualification Strategy

Benchmarq's goal is to provide the most reliable products possible. Hence, a combination of devices and packages representative of the front-end and back-end processes are selected for reliability testing. Three levels of qualification and reliability testing are performed on each product family. They are as follows:

Wafer Level

Wafer-level qualification is performed so that the reliability of the front-end process may be ascertained. Wafers from three front-end wafer lots are analyzed. Design rules such as critical dimensions, film thicknesses, step coverages, and oxide integrity are verified using a combination of electrical and visual analysis. Also, a series of tests designed to check the reliability of passivation, thin oxides, metal, and transistors are performed.

By analyzing the device in wafer form, any major process or design reliability problems are uncovered early in the product development phase where they can be more quickly corrected.

Package Level

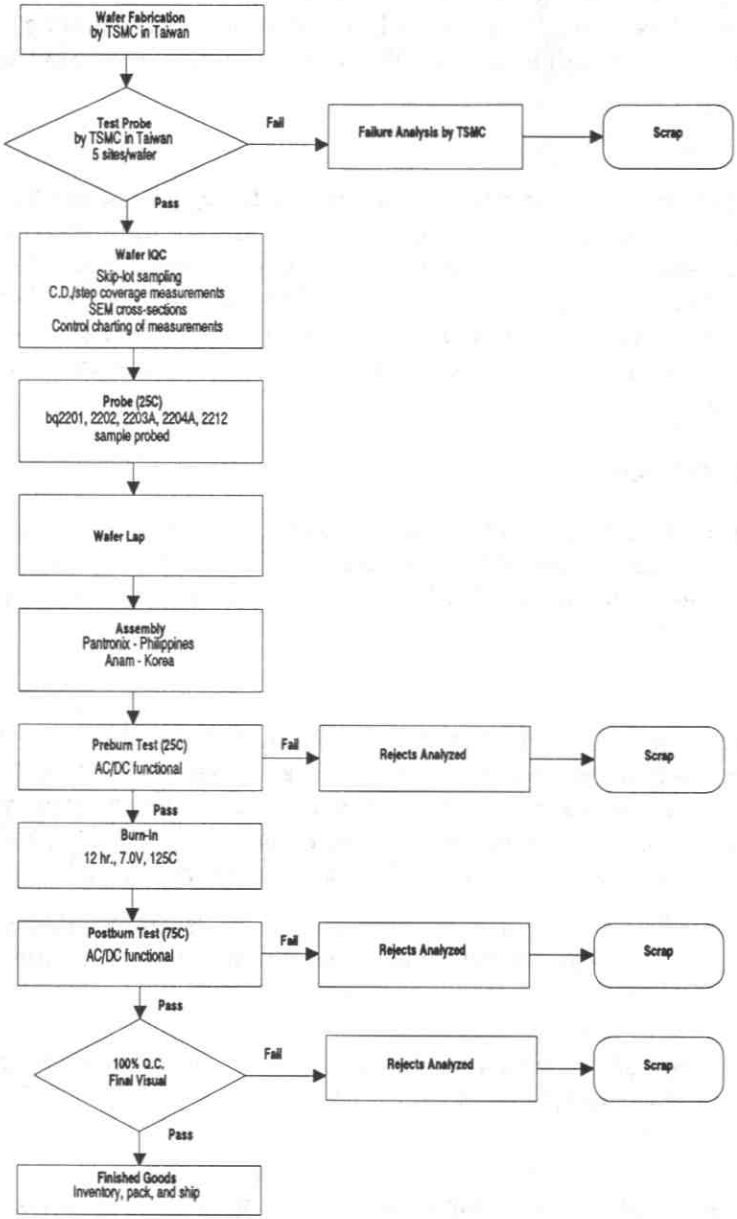
An assessment is performed on various package types to determine the reliability and manufacturability of the packaging process and materials.

System Level

Finally, a series of stringent environmental and operating life stresses are performed on packaged devices so that the short-term and long-term reliability of the product may be ensured. Infant life and long-term life predictions are then made based on this data.

NVSRAM Controllers

NVSRAM Controller Process Flow



Qualification Summary—NVSRAM Controllers

Product: NVSRAM Controllers (bq2201, bq2202, bq2204)

Qual Vehicle: bq2201SN 8-pin, 150-mil SOIC
(Lot: T044002AACPA Date Code: 9046)

High-Temperature Operating Life Test (5.5V, 150°C)

48 hrs	96 hrs	168 hrs
0/100	0/100	0/100

Operating Life Test (5.5V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/298	0/298	0/298	1/298 [1]	0/297

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/89	0/89	0/89	1/89 [1]	0/88

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/50	0/50	0/50	0/50	0/50

Highly Accelerated Stress Test—HAST (5.5V, 130°C, 85%RH, 1.7 atm)

24 hrs	48 hrs	72 hrs
0/50	0/50	0/50

Temperature Cycling (-65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/97 [1]	0/97	0/97

Thermal Shock (-55°C to 125°C)

30 cyc
0/50

Moisture Resistance (unbiased, -10°C to 65°C, 90%RH)

10 cyc
0/50

Resistance to Soldering Heat (260°C, 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/24 leads fail
Lead Fatigue	0/16 leads fail
Lead Finish	0/24 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 1000V
Latch-up Immunity	>± 200mA

[1]Refer to the August 1992 Benchmarq *Quality and Reliability Report.*

Predicted Failure Rates—NVSRAM Controllers

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (°K)
T_2	=	stress temperature (°K)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (based on 85°C/85% RH THB failure)
- Temperature derated to 55°C (typical use condition)

$AF_{(55°C - 125°C)} = 77.8$

$AF_{(55°C - 150°C)} = 259.9$

Total device hours:

bq2201 2000 hours x 298 devices x 77.8 = 46,368,800 device hours
bq2201 168 hours x 100 devices x 259.9 = 4,366,320 device hours
bq1001 1000 hours x 100 devices x 77.8 = 7,780,000 device hours

Total device hours = 5.8515×10^7 hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 1/5.815 \times 10^7 \text{ hours}$$

$$= 17.1 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 1
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures
α = 1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(4,\ 0.4)}}{2 \times (5.8515 \times 10^7)}$$

$$= 4.1175/(1.1703 \times 10^8)$$

$$= 3.52 \times 10^{-8}/\text{hours}$$

$$= 35.2 \text{ FITS}$$

Therefore, for the NVSRAM controllers built using the TSMC 1.2μ single-poly, double-level metal CMOS process, the mature life FIT rate is 36 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers a failure that occurs within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Derating for 150°C:

Infant life time	= AF x device stress hours
8760 hours	= 259.9 x device stress hours
Device stress hours	= 33.7 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life or in the first 33.7 hours of 150°C operating life is considered an infant life failure.

Total device hours:

bq2201 112.6 hours x 298 devices x 77.8 = 2,610,563 device hours
bq2201 33.7 hours x 100 devices x 259.9 = 875,863 device hours
bq1001 112.6 hours x 100 devices x 77.8 = 876,028 device hours

Total device hours = 4.3624×10^6 hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 4.3624 \times 10^6 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \text{ x total device hours}}$$

where:

f	=	number of failures
α	=	1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \text{ x } (4.3624 \text{ x } 10^6)}$$

$$= 1.8970 / (8.7249 \times 10^6)$$

$$= 2.174 \times 10^{-7} / \text{hours}$$

$$= 217.4 \text{ FITS}$$

Therefore, for the NVSRAM controllers built using the TSMC 1.2μ single-poly, double-level metal CMOS process, the infant life FIT rate is approximately 218 FITS.

NVSRAMs

NVSRAM Module Construction

Benchmarq's NVSRAM modules are designed and built by Benchmarq in Carrollton, Texas. Each module is constructed of one or more ICs mounted on a printed circuit board along with a lithium battery. This subassembly is then placed into a plastic housing and encapsulated with a specialized two-part epoxy. (The bq2502 Integrated Backup Unit is manufactured in the same manner.)

Quality Procedures

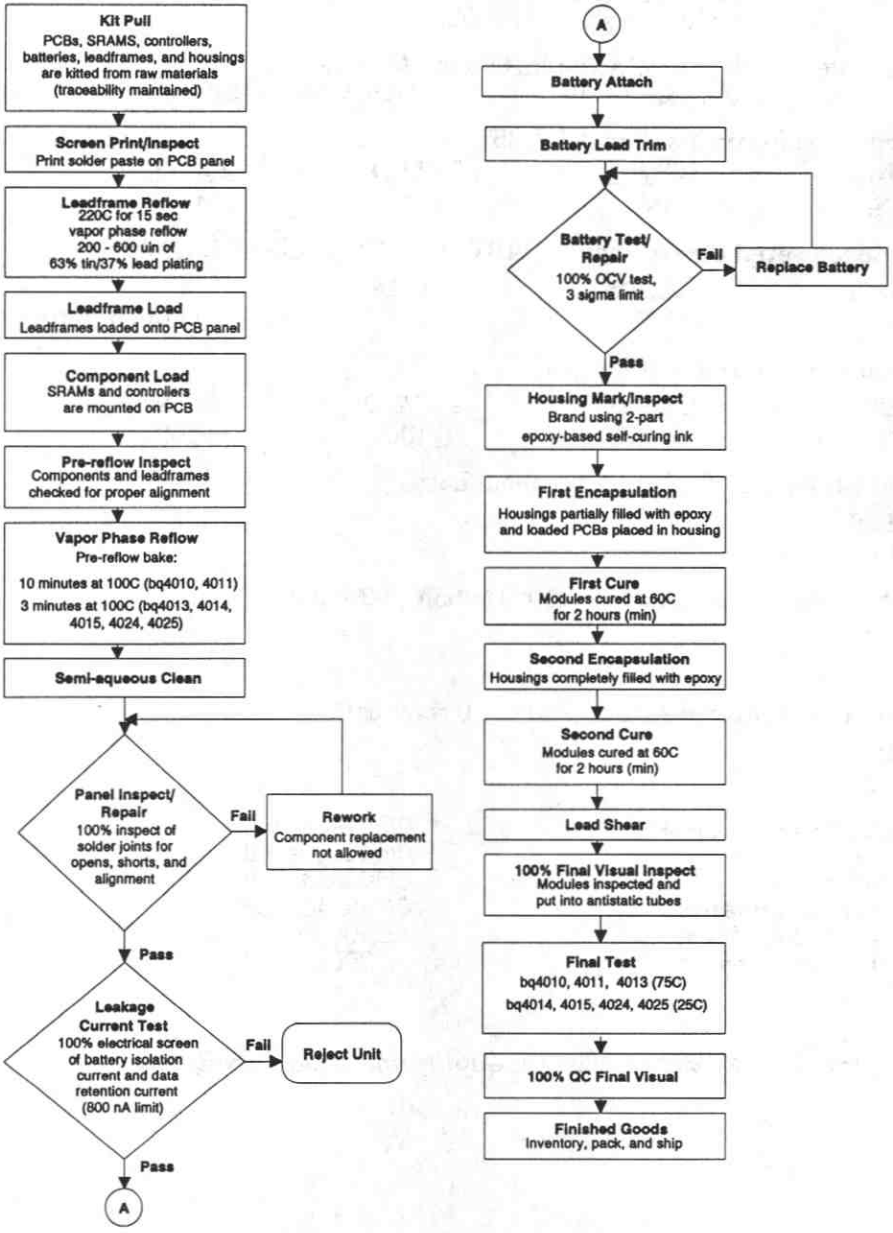
To help ensure that our final product is both consistent and reliable, the following quality inspections and tests are performed:

- **SRAMs**—Low-powered SRAMs are used in the manufacture of modules. At incoming inspection, data-retention current is measured on a representative sample from each lot. After the components are mounted on the circuit boards, the circuits are 100% tested for data-retention current.
- **Batteries**—Certificates of Compliance verifying the Open Circuit Voltage (OCV), Closed Circuit Voltage (CCV), and Internal Resistance (IR) are required from the manufacturer on each shipment. Historical statistical sampling indicates that a Lot Tolerant Percent Defective (LTPD) of less than 1% at a confidence level of 90% can be expected. After batteries are mounted on the circuit boards, they are 100% tested for OCV.
- **PCBs**—A sample from each lot of printed circuit boards is visually inspected for router damage, breakouts, opens, shorts, or misaligned solder masks.
- **Leads**—Certificates of Compliance verifying the plating thickness are required from the manufacturer. Periodic quality audits of the plating thickness are performed.

Traceability

Full traceability is maintained on both the integrated circuits and modules. The integrated circuits are traceable to front-end wafer lot and to assembly lot. The modules are traceable to housing, PCB, battery, controller, and SRAM lots.

NVSRAM Module Process Flow



Qualification Summary—NVSRAM Modules

Product NVSRAM Modules (bq4010, bq4011, bq4011H, bq4013, bq4014, bq4015, bq4024, bq4025, bq2502)

Qual Vehicle bq4010MA 28-pin, 600-mil Module
(Lot: QM04901 Date Code: 9049)

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/99	0/99	0/96 [1]	0/96	0/96

Highly Accelerated Stress Test*—HAST (5.5V, 130°C, 85%RH, 1.7 atm)

24 hrs	48 hrs	72 hrs
0/80	0/80	4/79 [1]

*(without battery)

Temperature Cycling (-40°C to +85°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100	0/100

Thermal Shock (-55°C to 125°C) without battery

30 cyc
0/105

Moisture Resistance (unbiased, -10°C to 65°C, 90%RH)

10 cyc
0/50

Resistance to Soldering Heat (260°C, 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/56 leads fail
Lead Fatigue	0/84 leads fail
Lead Finish	0/56 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 1000V
Latch-up Immunity	>± 200mA

[1] Refer to the August 1992 Benchmarq *Quality and Reliability Report.*

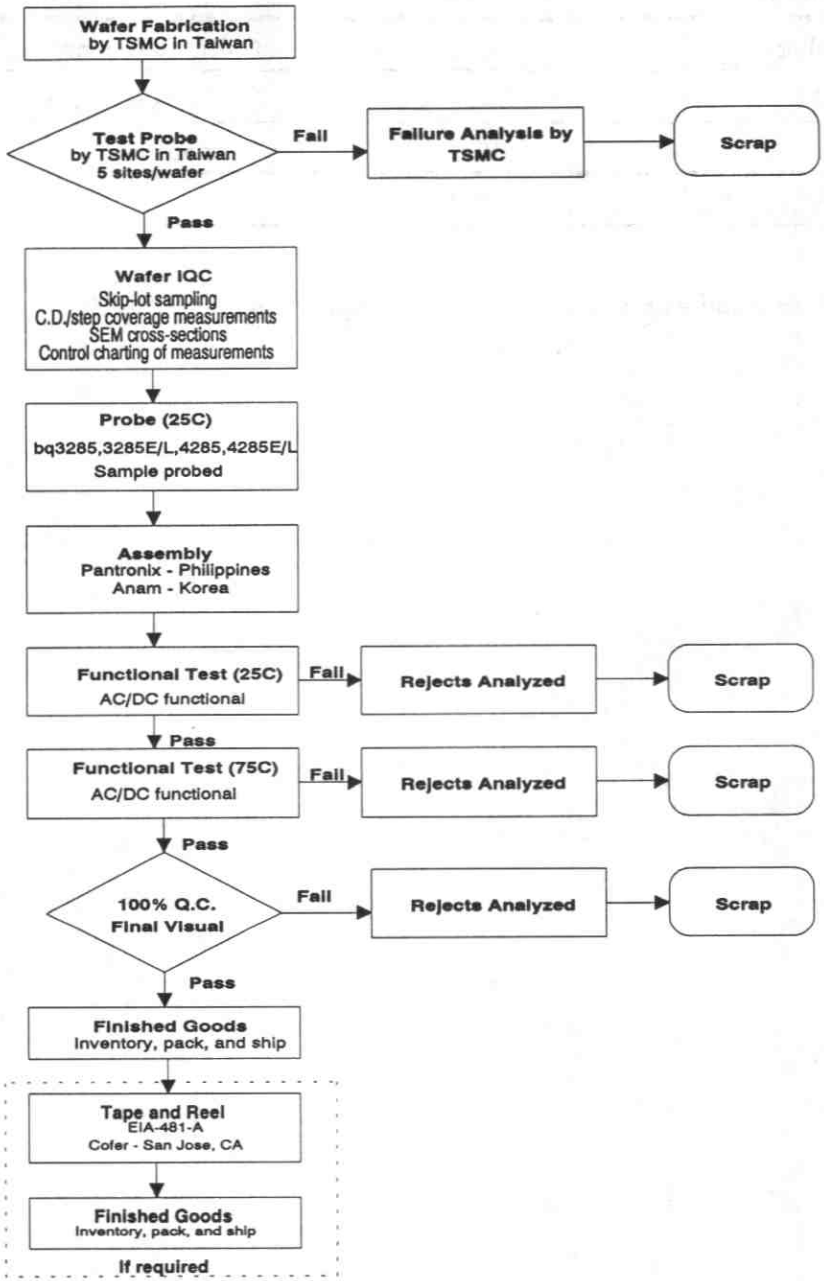
In the case of modules, an approximate FIT rate can be determined by adding together the FIT rates of the various components. The FIT rates used and their sources are listed below:

Component	FIT Rate	Source
Controller	36	Calculated in previous section
SRAM	35	SRAM manufacturer
Battery	<10	Panasonic (approximate)
Total	81 FITS	

Therefore, for our module products, the FIT rate is approximately 81 FITS.

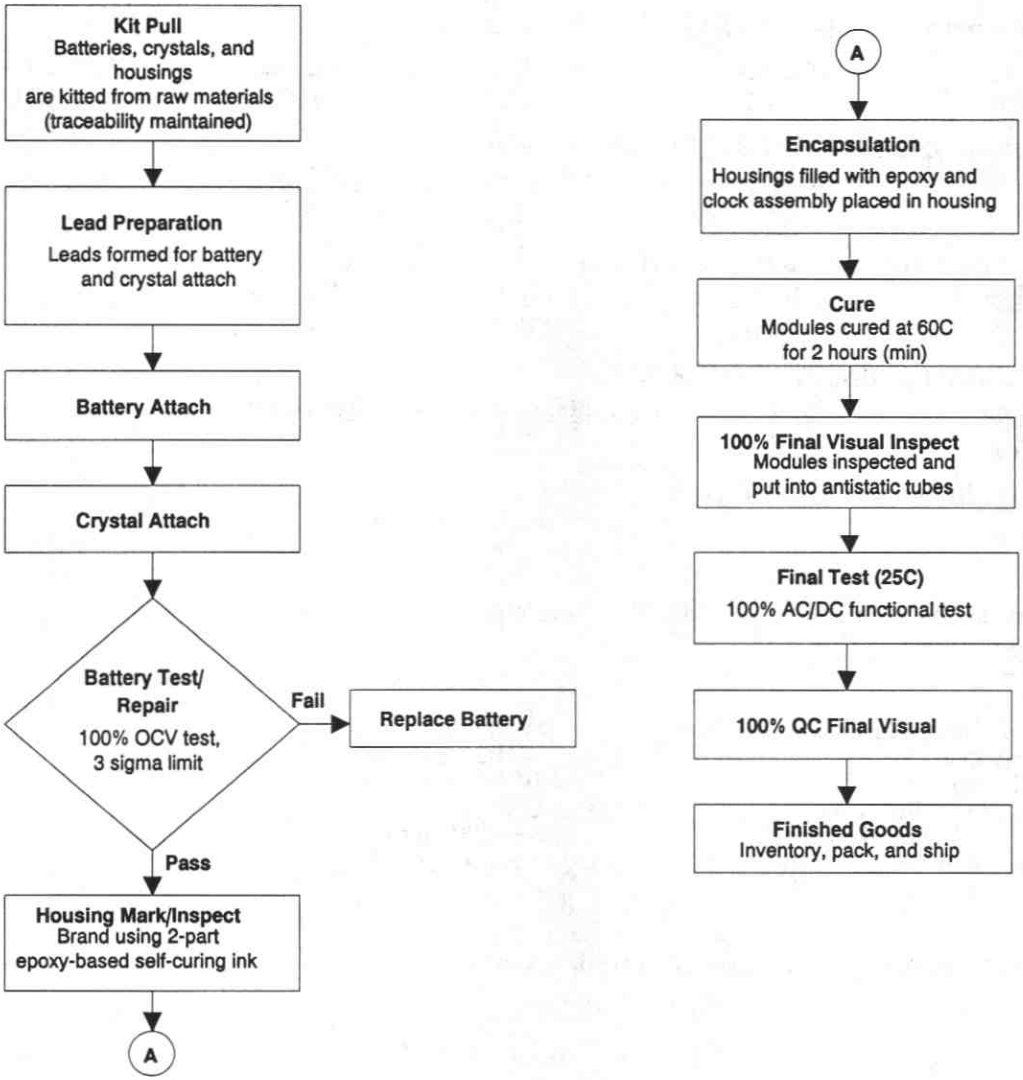
REAL-TIME CLOCKS (RTCs)

Real-Time Clock IC Process Flow



Real-Time Clock Module Process Flow

All modules are built by Benchmarq in Carrollton, Texas.



Qualification Summary-Real-Time Clock ICs

Product: RealTime Clocks (bq3285, bq3285E/L, bq4285, bq4285E/L)

Qual Vehicle: bq3285ES, 24pin 300mil SOIC

(Lot: 285AAEA, T346002, A61453.2 Date Code: 9332EP)

High-Temperature Operating Life Test (5.5V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/400	0/400	0/400	0/400	0/400

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/96	0/96	0/96	0/96	0/96

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/30	0/30	0/30	0/30	* 1/30

Temperature Cycling (65°C to +150°C)

100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/120 leads fail
Lead Fatigue	0/120 leads fail
Lead Finish	0/120 leads fail
Resistance to Solvents	0/5
Electrostatic Discharge	>±2000 volts
Latchup Immunity	>±200 mA

* Intermittent single bit failure—destroyed in analysis.

Qualification SummaryRealTime Clock Modules

Product: RealTime Clock Modules (bq3287, bq3287A, bq3287E, bq3287L, bq3287EA, bq3287LA, bq4287E, bq4287L)

Qual Vehicle: bq3287MT, 24pin 600mil Module

(Lot: QM147001 Date Code: 9147)

(Lot: PM205004 Date Code: 9205)

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/100	0/100	0/100	0/100	0/100

Highly Accelerated Stress Test HAST (5.5V, 130°C, 85%RH, 1.7 atm)

24 hrs	48 hrs	144 hrs
0/75	0/75	0/75

Temperature Cycling (65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/95

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/24 leads fail
Lead Fatigue	0/72 leads fail
Lead Finish	0/72 leads fail
Resistance to Solvents	0/4
Physical Dimension	0/4

Predicted Failure RatesRealTime Clock I.C.s

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (°K)
T_2	=	stress temperature (°K)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (conservative estimate)
- Temperature derated to 55°C (typical use condition)
- $AF_{(55°C - 125°C)} = 77.8$
- Voltage derated to 5.5V (typical use condition)
- $AF_{(5.5V - 7.0V)} = 5.0$ (conservative estimate)

Total device hours:

bq3285 2000 hours x 400 devices x 77.8 x 5.0 = 311,200,000 device hours

Total device hours = 3.1120×10^8 hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 3.1120 \times 10^8 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 0

Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \text{ x total device hours}}$$

where:

f = number of failures

α= 1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \text{ x } (1.2448 \text{ x } 10^8)}$$

$$= 1.8970 / (6.224 \text{ x } 10^8)$$

$$= 3.05 \text{ x } 10^{-9} / \text{hours}$$

$$= 3.05 \text{ FITS}$$

Therefore, for the real-time clock integrated circuit built using the TSMC 0.8µ CMOS single-poly, double-level metal process, the mature life FIT rate is approximately 3 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers failures that occur within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life is considered an infant life failure.

Total device hours:

bq3285 112.6 hours x 400 devices x 77.8 x 5.0 = 17,520,560 device hours

Total device hours = 1.7520×10^7 hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 1.7520 \times 10^7 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

Number of failures: 0

Confidence level: 60%

where:

f = number of failures

α= 1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (7.0082 \times 10^6)}$$

$$= 1.8970 / (3.5041 \times 10^7)$$

$$= 5.4136 \times 10^{-8} / \text{hours}$$

$$= 54.1 \text{ FITS}$$

Therefore, for the real-time clock integrated circuit built using the TSMC 0.8 single-poly, double-level metal CMOS process, the infant life FIT rate is approximately 54 FITS.

Predicted Failure Rates RealTime Clock Modules

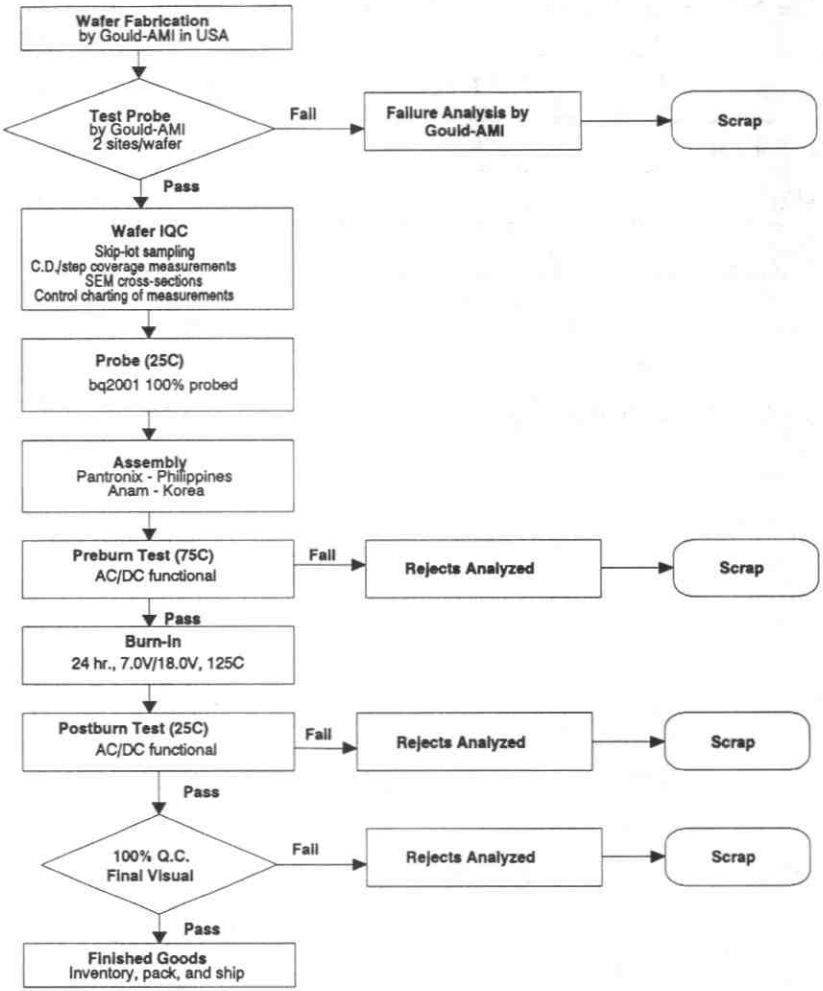
In the case of modules, an approximate FIT rate can be determined by adding together the FIT rates of the various components. The FIT rates used and their sources are listed below:

Component	FIT Rate	Source
Real-Time Clock IC	3	Calculated in previous section
Crystal	<5	Daiwa (approximate)
Battery	<2	Panasonic (approximate)
Total	10 FITS	

Therefore, for our RTC module products, the FIT rate is approximately 10 FITS.

Energy Management Units (EMUs)

Energy Management Unit Process Flow



Qualification Summary-Energy Management Units

Product: Energy Management Unit (bq2001)

Qual Vehicle: bq2001, 24-pin 300-mil SOIC
(Lot: A129001ABCK, A135001ADQK, A135001AEEK, A135001AJCA, A137002AACA, A206003ABCA)
(Date Code: 9130, 9135, 9136, 9141, 9141, 9208)

High-Temperature Operating Life Test (5.5V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/300	0/300	0/300	0/300	0/300

High-Temperature Operating Life Test (7.0V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/84	0/84	0/84	0/84	0/84

Temperature/Humidity/Bias (7.0V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/100	0/100	0/100	0/100	0/100

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/50	0/50	0/50	0/50	0/50

Highly Accelerated Stress Test - HAST (5.5V, 130°C, 85%RH, 1.7 atm)

48 hrs	96 hrs	168 hrs
0/99	0/99	0/99

Temperature Cycling (-65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	1/100[1]	0/99	0/99	1/99[1]

Thermal Shock (-55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/10

Solderability (245°C, 5 seconds)	0/168 leads fail
Lead Fatigue	0/72 leads fail
Lead Finish	0/72 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 2000 volts
Latch-up Immunity	>± 200 mA

[1] Refer to the August 1992 Benchmarq *Quality and Reliability Report.*

Predicted Failure Rates—Energy Management Units

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (°K)
T_2	=	stress temperature (°K)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (conservative estimate)
- Temperature derated to 55°C (typical use condition)

  $AF_{(55°C - 125°C)} = 77.8$

- Voltage derated to 5.5V (typical use condition)

  $AF_{(5.5V - 7.0V)} = 5.0$ (conservative estimate)

Total device hours:

bq2001 2000 hours x 300 devices x 77.8 = 46,680,000 device hours
bq2001 2000 hours x 84 devices x 77.8 x 5.0 = 65,352,000 device hours

Total device hours = 1.1203×10^8 hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 1.1203 \times 10^{8} \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2f + 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures
α = 1 – confidence level

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (1.1203 \times 10^{8})}$$

$$= 1.8970 / (2.2406 \times 10^{8})$$

$$= 8.4663 \times 10^{-9} / \text{hours}$$

$$= 8.5 \text{ FITS}$$

Therefore, for the EMUs built using the Gould-AMI 1.5µ BiCMOS process, the mature life FIT rate is approximately 9 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers failures that occur within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life is considered an infant life failure.

Total device hours:

bq2001 112.6 hours x 300 devices x 77.8 = 2,628,084 device hours
bq2001 112.6 hours x 84 devices x 77.8 x 5.0 = 3,679,320 device hours

Total device hours = 6.3074×10^6 hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 6.3074 \times 10^6 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

Number of failures: 0
Confidence level: 60%

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f	=	number of failures
α	=	1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (6.3074 \times 10^6)}$$

$$= 1.8970 / (1.2615 \times 10^7)$$

$$= 1.5038 \times 10^{-7} / \text{hours}$$

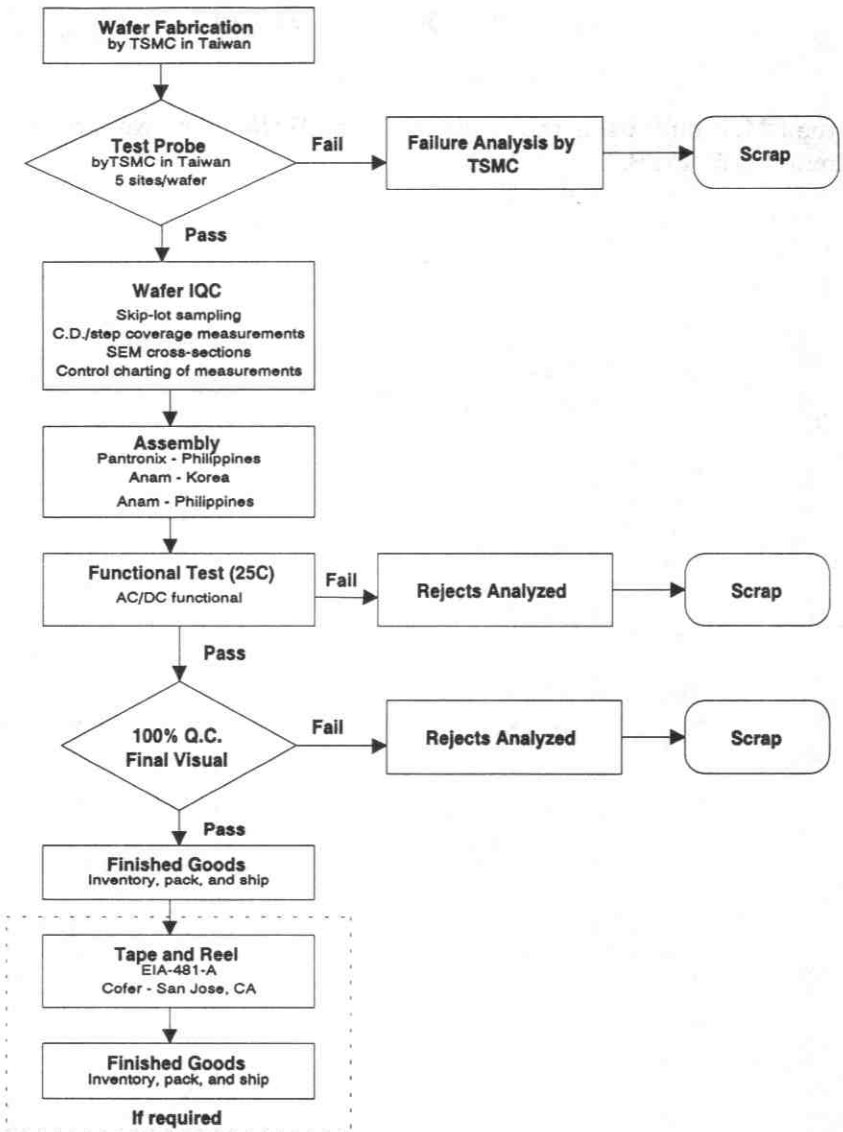
$$= 150.4 \text{ FITS}$$

Therefore, for the EMUs built using the Gould-AMI 1.5μ BiCMOS process, the infant life FIT rate is approximately 151 FITS.

Battery Management ICs

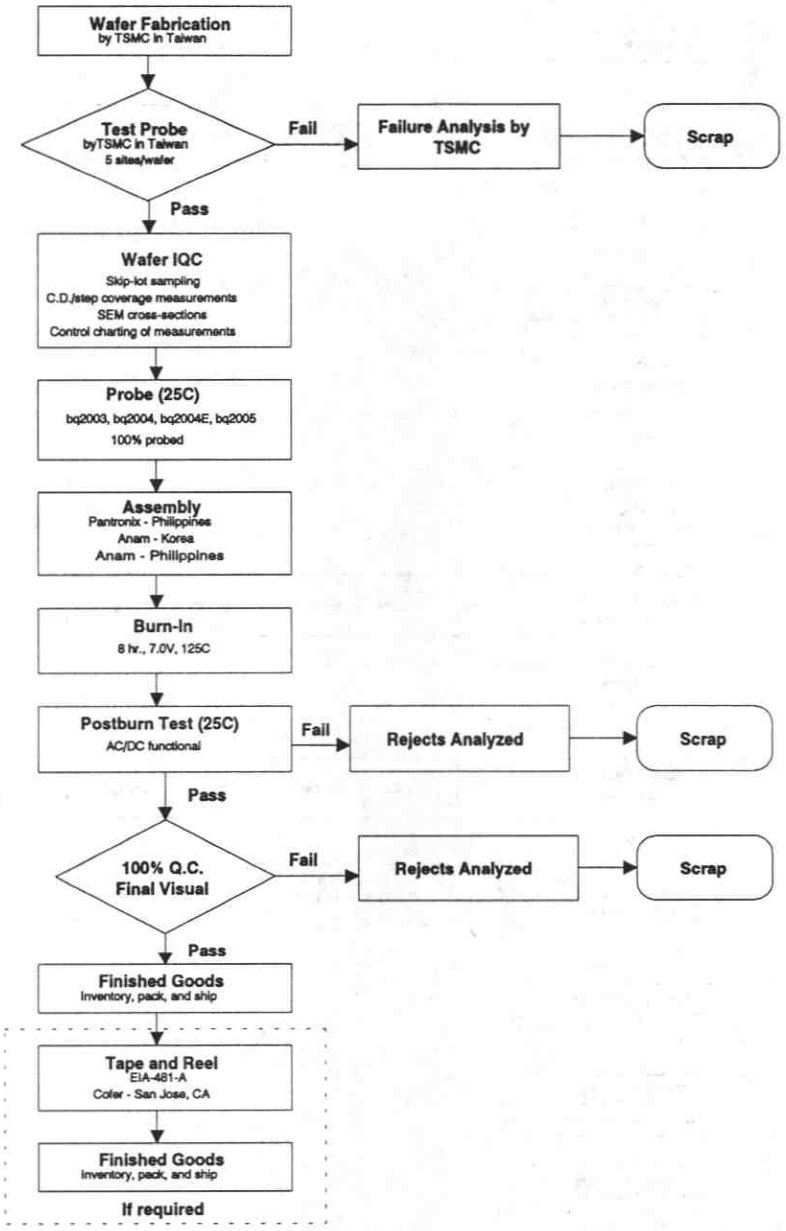
bq2002, bq2007 Fast Charge IC Process Flow

bq2002, 2007 Fast Charge IC Process Flow



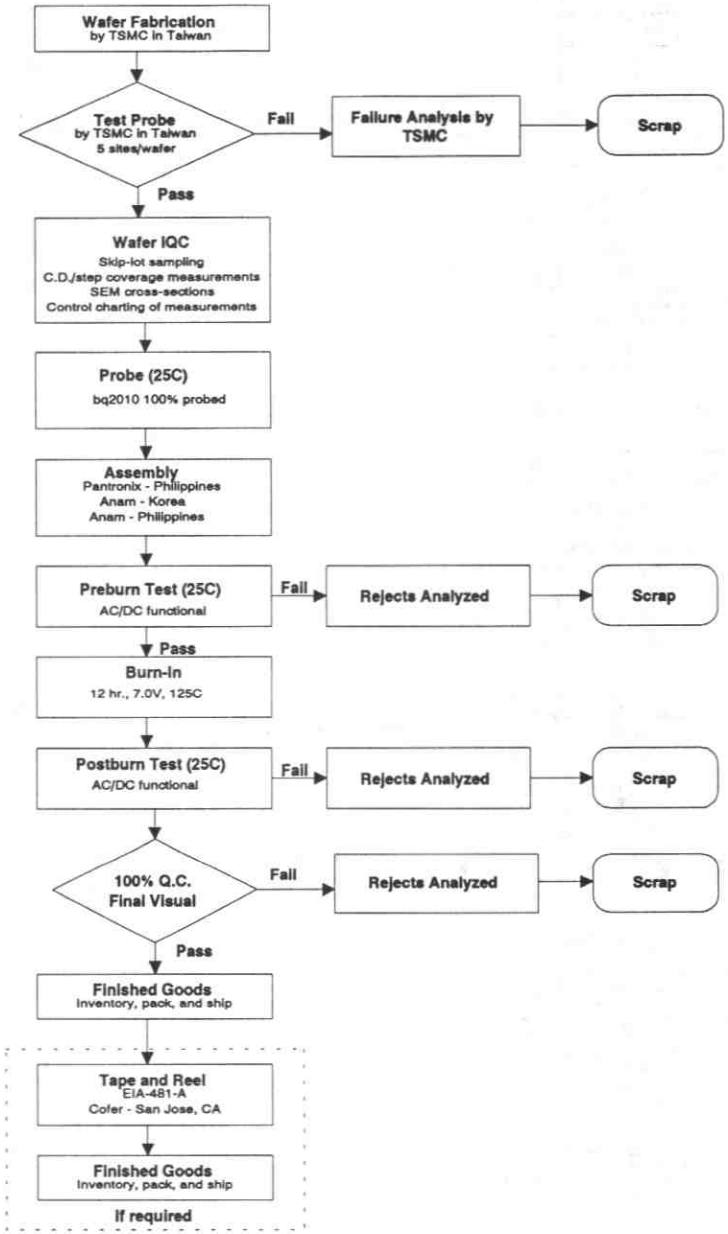
bq2003, 2004, 2004E, 2005 Fast Charge IC Process Flow

bq2003, 2004, 2004E, 2005 Fast Charge IC Process Flow



bq2010 Gas Gauge IC Process Flow

bq2010 Gas Gauge IC Process Flow



Qualification Summary—Fast Charge IC

Product: bq2003 Fast Charge IC

Qual Vehicle: 20-pin 300-mil PDIP

(Lots: T221001, T237001, T244012)

(Lot: 211ABCP Date Code: 9226-EP)

High-Temperature Operating Life Test (7.0V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/399	0/399	0/399	0/399	0/399

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/120	0/120	0/120	0/120	0/120

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs	2000 hrs
0/50	0/50	0/50	0/50	0/50

Temperature Cycling (65°C to +150°C)

10 cyc	100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/96 leads fail
Lead Fatigue	0/80 leads fail
Lead Finish	0/80 leads fail
Resistance to Solvents	0/4 devices fail
Electrostatic Discharge	>± 2000 volts
Latchup Immunity	>± 200 mA

Qualification Summary—Dual-Battery Fast Charge IC

Product: bq2005 Dual-Battery Fast Charge IC

Qual Vehicle: 20-pin 300-mil SOIC

(Lot: 232AACA Date Code: 9329)

High-Temperature Operating Life Test (7.0V, 125°C)

48 hrs	168 hrs	500 hrs	1000 hrs
0/144	0/144	0/144	0/144

Temperature/Humidity/Bias (5.5V, 85°C, 85%RH)

48 hrs	168 hrs	500 hrs	1000 hrs
0/99	0/99	0/99	0/99

High-Temperature Storage (unbiased, 150°C)

48 hrs	168 hrs	500 hrs	1000 hrs
0/50	0/50	0/50	0/50

Temperature Cycling (65°C to +150°C)

100 cyc	300 cyc	600 cyc	1000 cyc
0/100	0/100	0/100	0/100

Thermal Shock (55°C to +125°C)

30 cyc
0/50

Resistance to Soldering Heat (260°C , 10 seconds)

1 cyc
0/5

Solderability (245°C, 5 seconds)	0/100 leads fail
Lead Fatigue	0/100 leads fail
Lead Finish	0/100 leads fail
Resistance to Solvents	0/5 devices fail
Electrostatic Discharge	>± 2000 volts
Latchup Immunity	>± 200 mA

Predicted Failure Rates—Fast Charge ICs

Most integrated circuit failure mechanisms are based on physical or chemical reactions. These reactions are accelerated by temperature and can be modeled using the Arrhenius equation. The acceleration factor (AF) between any two temperatures may be calculated as follows:

$$AF_{(T_1 - T_2)} = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where:

AF	=	acceleration factor
e	=	natural log
E_a	=	activation energy in electron volts
k	=	Boltzman's constant (8.62×10^{-5} eV/°K)
T_1	=	derated temperature (°K)
T_2	=	stress temperature (°K)

The following assumptions have been made in Benchmarq's determination of failure rates:

- Activation energy = 0.7 eV (conservative estimate)
- Temperature derated to 55°C (typical use condition)
- $AF_{(55°C - 125°C)} = 77.8$
- Voltage derated to 5.5V (typical use condition)
- $AF_{(5.5V - 7.0V)} = 5.0$ (conservative estimate)

Total equivalent device hours:

bq2003 2000 hours x 399 devices x 77.8 x 5.0 = 310,422,000 device hours
bq2005 1000 hours x 144 devices x 77.8 x 5.0 = 56,016,000 device hours

Total equivalent device hours: 366,438,000 device hours

A single-point estimate of the mature life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 3.66438 \times 10^8 \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the mature life failure rate can be made using the following information:

Number of failures: 0

Confidence level: 60%

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures

α = 1 – confidence level

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (3.10422 \times 10^8)}$$

$$= 1.8970 / (7.32876 \times 10^8)$$

$$= 2.59 \times 10^{-9} / \text{hours}$$

$$= 2.6 \text{ FITS}$$

Therefore, for the Battery Management ICs built using the TSMC 1.2µ double-level poly, double-level metal CMOS process, the mature life FIT rate is approximately 3 FITS.

A similar determination of the infant life failure rate can be made. Benchmarq considers failures that occur within 1 year (8760 hours) at normal operating conditions an infant life failure.

Derating for 125°C:

Infant life time	= AF x device stress hours
8760 hours	= 77.8 x device stress hours
Device stress hours	= 112.6 hours

Therefore, any failure that occurs in the first 112.6 hours of 125°C operating life is considered an infant life failure.

Total equivalent device hours:

bq2003 112.6 hours x 399 devices x 77.8 x 5.0 = 17,476,759 device hours
bq2005 112.6 hours x 144 devices x 77.8 x 5.0 = 6,307,402 device hours

Total equivalent device hours: 23,784,161 device hours

A single-point estimate of the infant life failure rate may be calculated as follows:

$$\text{Failure rate} = \frac{\text{number of failures}}{\text{total device hours}}$$

$$= 0 / 2.3784 \times 10^{7} \text{ hours}$$

$$= 0 \text{ FITS}$$

Next, a Chi square approximation of the infant life failure rate can be made using the following information:

Number of failures: 0

Confidence level: 60%

$$\text{Failure rate} \left(\chi^2 \right) = \frac{\chi^2_{(2f\ +\ 2,\ \alpha)}}{2 \times \text{total device hours}}$$

where:

f = number of failures

α = 1 – confidence level

$$\text{Failure rate}\left(\chi^2\right) = \frac{\chi^2_{(2,\ 0.4)}}{2 \times (1.7477 \times 10^7)}$$

$$= 1.8970 / (4.7568 \times 10^7)$$

$$= 3.9880 \times 10^{-8} / \text{hours}$$

$$= 39.9 \text{ FITS}$$

Therefore, for the Battery Management ICs built using the TSMC 1.2μ double-level poly, double-level metal CMOS process, the infant life FIT rate is approximately 40 FITS.

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